

High temperatures solder replacement to meet RoHS

**C HUNT, L CROCKER, O THOMAS, M WICKHAM, K CLAYTON,
L ZOU, R ASHAYER-SOLTANI, A LONGFORD**

APRIL 2014

High temperatures solder replacement to meet RoHS

C Hunt¹, L Crocker¹, O Thomas¹, M Wickham¹, K Clayton¹,
L Zou¹, R Ashayer-Soltani¹, A Longford²

¹ National Physical Laboratory, UK

² PandA Europe, UK

ABSTRACT

This project has considered the effect of removal of exemptions to RoHS, specifically the future loss of the ability to use high melting point solders that are based on alloys that typically have 90% lead composition. We have looked at the impact of the ban of this alloy and the response in the industry and the market place. While multiple solutions have been found, the authors have considered the use of sintered silver as a viable solution and a strong favourite. A review of the literature is reported. We have undertaken a first pass at assembly techniques and evaluation of interconnects, and we report the results of single component type assemblies, which were aged and then tested. Testing also included full mechanical testing, and an evaluation of a proto-type hot shear test method. This project has identified important characteristics of the sintered silver system, and metrology challenges that need to be addressed.

© Queens Printer and Controller of HMSO, 2014

ISSN 1754-2979

National Physical Laboratory
Hampton Road, Teddington, Middlesex, TW11 0LW

Extracts from this report may be reproduced provided the source is acknowledged and the extract is not taken out of context.

Approved on behalf of NPLML by Dr M Gee,
Knowledge Leader, Materials Team.

CONTENTS

1.	INTRODUCTION	1
2.	EXPERIMENTAL.....	2
3.	TEST METHODOLOGY	5
4.	RESULTS	7
5.	DISCUSSION.....	14
6.	CONCLUSIONS	16
7.	REFERENCES:	16

1. INTRODUCTION

Electronic circuit assemblies are ubiquitous, and are a contingent part of an incredibly wide range of products and applications. A common feature of electronic assemblies is that the components are attached with solder, a tin based alloy. The 2006 RoHS “The Restriction of the Use of Certain Hazardous Substances in Electrical and Electronic Equipment Regulations” restricted the use of lead, which resulted in a new family of solder compositions. There were however exemptions, and paradoxically an alloy with >85% lead was allowed because of its high melting point, and there being no known alternatives.

In 2013 RoHS was recast with modified restrictions and new exemptions and importantly, it stated for the first time that all exemptions will automatically expire after 5 or 7 years, unless they are renewed. This has put a lot of pressure on industry, which need certainty in their product portfolios over long time periods. One of the exemption’s, 7(a) “lead in high melting temperature type solders (i.e. lead based alloys containing 85% by weight or more of lead), could therefore be lost. These high temperature solders have long been used in hierarchical soldering for attaching silicon die within components. Furthermore, there has been an increase in the demand for high temperature interconnect solutions at circuit board level joining with recent introductions of high power semiconductors and increased operating temperatures. Application areas for these new devices include the electric vehicle, renewable energy, avionics and oil and gas. Annex A deals in detail with the likely impact of the loss of the high temperature lead alloy exemption.

Economic replacement material solutions for high Pb alloys are currently being sort, and alternatives are high temperature conductive adhesives, sintered materials, and transient liquid phase solders. While these new materials are becoming available independent verification of their properties has not been established, and problems associated with processing and lifetime have yet to be resolved. Furthermore their initial introduction is not targeted at the attachment of electronics components to substrates. These materials are being sold for die attach within packages. A significant advantage of the sintered silver as a component interconnect, is that once formed, it will not soften again until the melting point is achieved at 960 °C. It is this property that makes the silver solution stand out, as it is the clear favourite to meet the interconnection road block posed by silicon carbide, and unlock the transition to truly high temperature electronics operating above 300 °C.

The new material solutions behave differently to solders, due to their composition and structure and hence there is a need for new test regimes that are relevant to their degradation mechanisms. How these new material interconnects degrade is not fully understood and bespoke testing needs to be developed. Furthermore, since the application areas in circuit boards are at higher temperatures than hitherto, there will be a commensurate need to increase the testing temperature capability. This requirement for increased interconnect characterisation temperatures is beyond current capability and presents some difficult challenges. This project has attempted to use a modification of existing equipment as a first step in understanding the complexities in the metrology challenges for high temperature interconnects.

Sintered silver is provided commercially as a paste, and hence is similar to solder paste in how it can be handled. Typically for both material types, they are stencil printed and then heated to form the interconnect, removing the liquid phase in the process. Solder pastes contain fluxes, sintered silver pastes do not. However, the silver pastes typically contain high boiling point alcohols which decompose to form CO₂ and H₂O, which in turn produces carbonic acid and helps to remove silver oxide and hence aid the sintering process.

This project has made initial measurements using a commercially available sintered silver interconnect, which offers the best solution for replacing the lead tin solder. A review is presented of the current research into the use of sintered silvers, and is given in Annex B.

Sintering in its widest sense requires elevated temperatures, pressure and time. During sintering, individual particles undergo solid state diffusion and agglomerate into a single continuous material. Sufficient temperature, pressure and time are needed to ensure complete consolidation to remove porosity, so that the full bulk properties are achieved. For electronic component attachment, high temperature and pressure present some difficult challenges, and long process times are undesirable. This dichotomy is conveniently avoided since the full bulk properties are not required. All that is required is to attach the component to the substrate and this is not mechanically demanding. Furthermore, a material with porosity can be speculated to have superior compliance and out-perform a 100% solid in repetitive shear cycles, since the pores provide a network of compressible space. However, such a material will not necessarily be stable and consolidation and removal porosity may be expected over time.

In this project we have attached ceramic chip resistors to two types of high temperature substrate. We have also produced single lap shear joints using silver bar as a substrate. A fabrication process for the samples has been developed and these have then been conditioned and tested. The applied conditioning comprised hot ageing and thermal cycling. The testing comprised electrical continuity, shear testing and instrumented isothermal mechanical testing. An initial foray into high temperature testing was evaluated by developing and mounting a high temperature stage onto the NPL commercial shear testing instrument.

This preliminary investigation also considered what future developments are needed for a complete metrology approach to characterising interconnects performing at high temperature.

2. EXPERIMENTAL

The sinter paste material used in this project was a commercial silver paste. Three specimen types were produced; (i) an assembly with multiple ceramic resistors mounted on a substrate for thermal cycling, electrical monitoring and shear testing, (ii) a single lap joint for mechanical testing and (iii) a single ceramic resistor mounted on a substrate for hot shear testing.

The assembly test vehicles

Multiple Component PCB Test Vehicles: Two types of ceramic resistors that only differed by the termination finish, a special finish of platinum on silver and was purchased from Rhopoint Components; the other was a tin finished component with a slightly larger pad size. Two substrate materials were evaluated the first was a polyimide with an electroless nickel, electroless palladium, immersion gold (ENEPIG) finish, the second a composite PTFE ceramic substrate with the same finish. These are shown in Figure 1. They were supplied by Invotec and Stevenage Circuits respectively. The test vehicles were designed to enable shear and 4 probe resistance measurements. The substrate materials were capable of being aged at temperatures up to 250 °C. The PTFE ceramic substrate is rated up to 300 °C, whereas the polyimide substrate is capable up to 250 °C for limited time durations and only rated to 200 °C for continuous lifetime exposure. The tin finished components were paired with the polyimide, and are typical of current day material set for running up to 200 °C, and the platinum on silver with the PTFE ceramic pair represent a higher temperature performance option. Examples of cross sections of the two sets are shown in Figures 2 and 3.

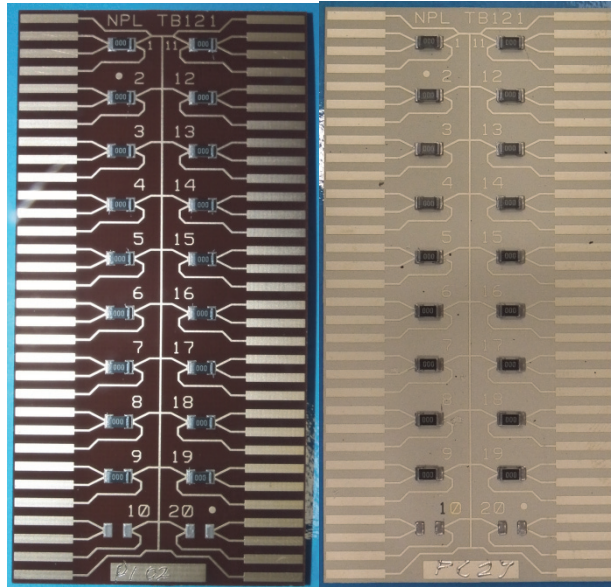


Figure 1: Multiple component test vehicles on polyimide (left) and composite PTFE ceramic (right)

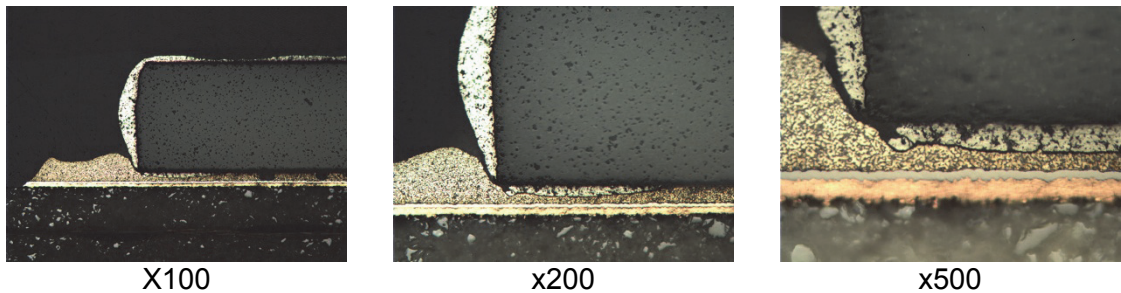


Figure 2: As manufactured PtAg finished components assembled at 300 °C for 30mins

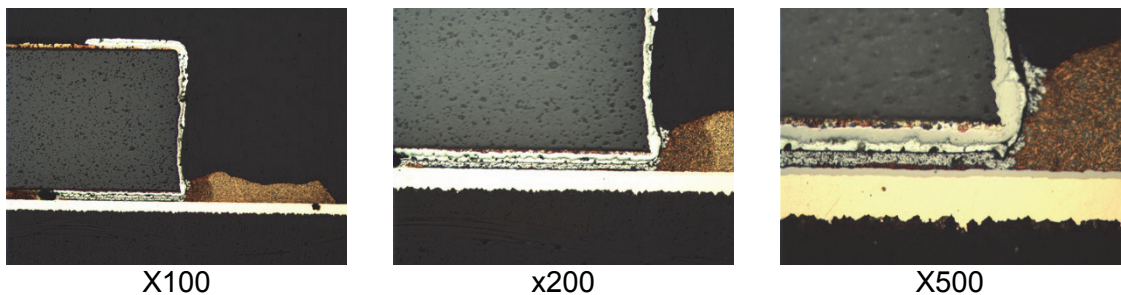


Figure 3: As manufactured Sn finished components assembled at 230 °C for 5 mins

These conditions were selected after some exploratory testing. The above conditions were beyond our initial expectations, as previous client based work had shown that lower temperatures were feasible. It was not clear where the differences arose from; there were minor material differences, but these were not expected to be problematic. The above conditions did prove satisfactory and were within the material suppliers recommended processing parameters.

The following assembly process was followed. The silver paste was allowed to reach room temperature and mixed thoroughly before use. A 265GSx DEK stencil printer was used to print the boards using a 75 μm stencil, 10 mm/s print speed and 3 Kg print pressure. The printed boards were mounted onto the Goldplace L40 automatic pick and place system and assembled with 18 R1206 components of tin or platinum/silver terminations. The sintering profile included a drying stage in which the assembled boards were placed in an oven at room temperature and gradually heated to a set temperature of 165 °C. Once the set temperature was reached the boards remained drying at 165 °C for 1 hour.

The poly-ceramic substrates assembled with platinum silver components were sintered at 300 °C for 30 minutes and the polyimide substrates with tin components were sintered at 230 °C for 5 minutes. For both assemblies, no pressure was applied to the component during assembly.

Single Lap Joint Test Vehicle: The single lap joint, shown schematically in Figure 3, was constructed using silver arms, each $30 \times 5 \times 0.6$ mm, that were pre-etched with a commercial alkaline solution before assembly. The paste was printed through a 100 μm stencil with a 5×1 mm aperture. Each arm was printed with the paste deposit, dried at 165 °C for 1 hour, and then sintered at 275 °C under a pressure of 2 MPa. The final joint height was 70 ± 25 μm .



Figure 3: Schematic of single lap joint

Single Component Hot Shear Test Vehicles: These consisted of a zero ohm tin finished 2512 resistor mounted on a FR4 substrate with an ENIPIG finish. The temperature profile for making the joints was to first ramp to 165 °C in one minute, hold for 2 minutes during which a force (27 ± 1 N was applied) before ramping up to the higher temperature (240 ± 15 °C) and holding it for 3 minutes. After which, the heater is turned off and the sample and jig allowed to cool. As soon as the sample starts to cool, the force is removed. In Figure 10 the sample can be heated, and as shown various parts of the apparatus are instrumented with thermal couples.

A further four samples were made using a silver substrate and a silver coupon to simulate the component. The same stencil and paste were used as for the R2512 component samples. These were then stuck to the FR4 coupons with high temperature adhesive (Scotch Weld DP760) to allow mounting into the hot shear tester. The arrangement is shown in Figure 5.

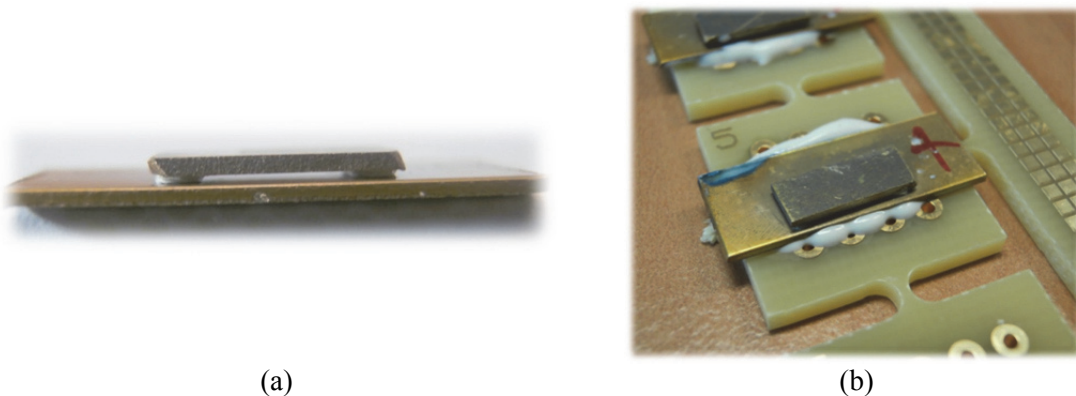


Figure 5: A silver sample mounted with sintered silver on a silver substrate (a), and then mounting this on a FR4 substrate with an adhesive (b).

3. TEST METHODOLOGY

Shear testing: The shear tester was a Dage Series 4000, with a DS 100Kg testing head. The stand-off height of the chisel tool above the PCB surface was 80 μm . During each test, the shear tool was moved forward at a defined speed of 200 $\mu\text{m/s}$ against the test component, and the force was monitored until the solder joint broke. A typical arrangement is shown in Figure 6.

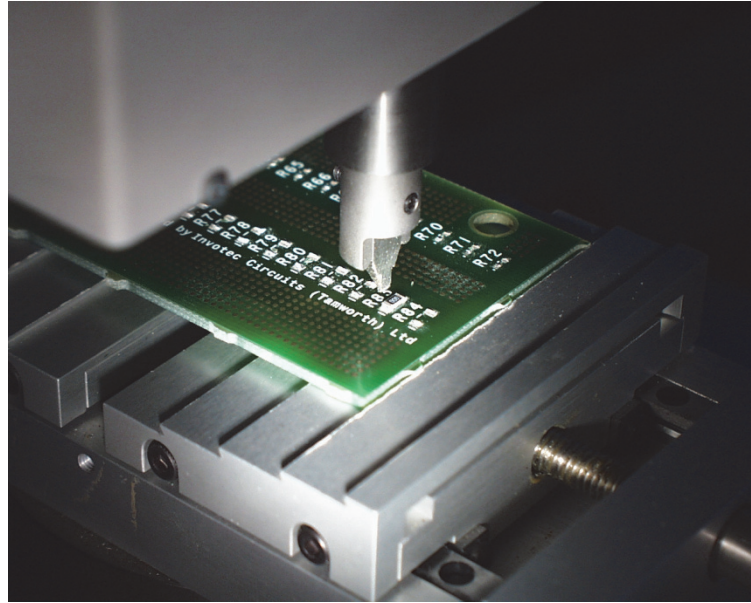


Figure 6: Shear test jig and push-off tool

Mechanical Testing: Mechanical testing of the sintered silver samples was carried out in the Interconnect Properties Testing Machine (IPTM)⁽¹⁾ shown in Figure 7. This machine is able to accurately control applied displacement to an interconnect whilst measuring the supported load. Spacers are used with the single lap sample geometry to ensure that the sample axis is in line with the IPTM and not rotated.

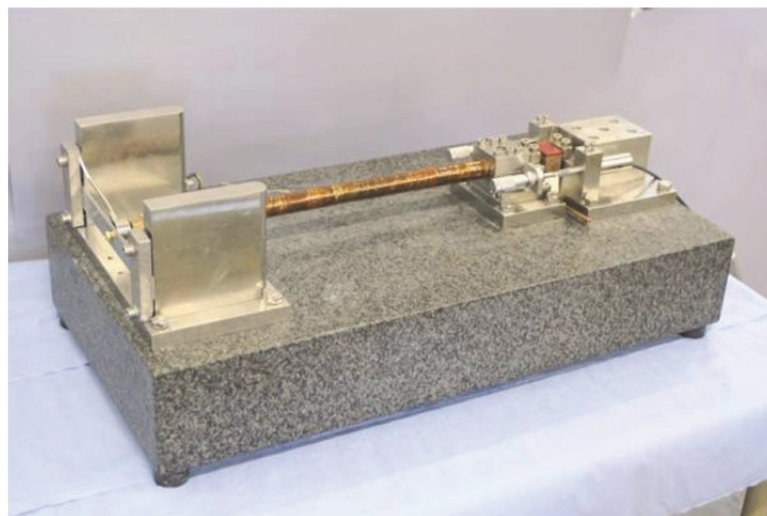


Figure 7: Interconnect Properties Testing Machine (IPTM)

Two loading regimes were used with the IPTM. Firstly an increasing cyclic displacement range with a constant cycle time, and secondly a constant displacement range of $\pm 30 \mu\text{m}$. Both measurements were performed at ambient, 22°C . The cyclic displacement parameters were a 20 minute cycle with displacement amplitudes of 3 microns and 200 second dwells. After two cycles at this amplitude, the amplitude was increased further in steps up to 40 microns amplitude. This waveform is shown in Figure 8.

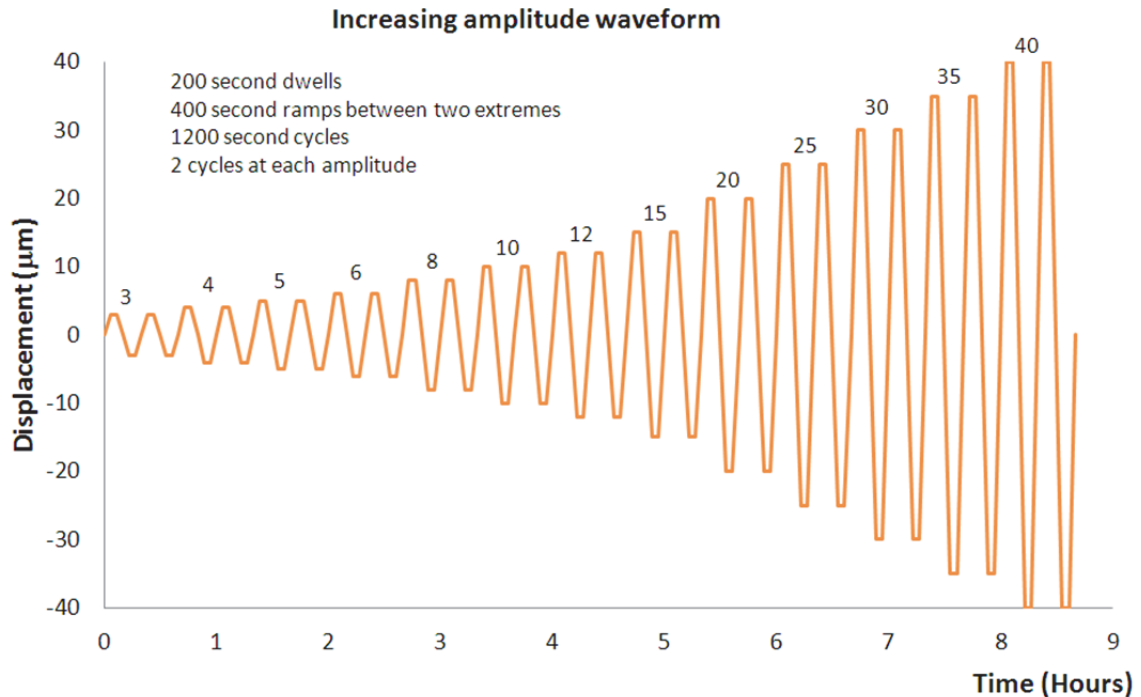


Figure 8: Increasing amplitude waveform applied using the IPTM

Some samples were selected for fatigue experiments. A 20 minute cycle was applied with 200 second dwells as shown in Figure 9. Samples were tested with a waveform amplitude of 20, 30 and $40 \mu\text{m}$

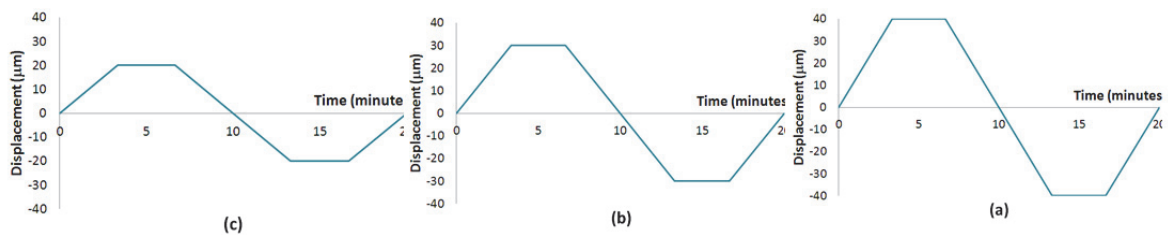


Figure 9: Fatigue waveforms for 20, 30 and $40 \mu\text{m}$ amplitudes

Hot shear testing: Typically shear testing is undertaken at ambient, however by modification of the shear tester, and incorporation of a heater stage, shear could be undertaken at elevated temperatures. A close up of the mounted heater stage is shown in Figure 10.

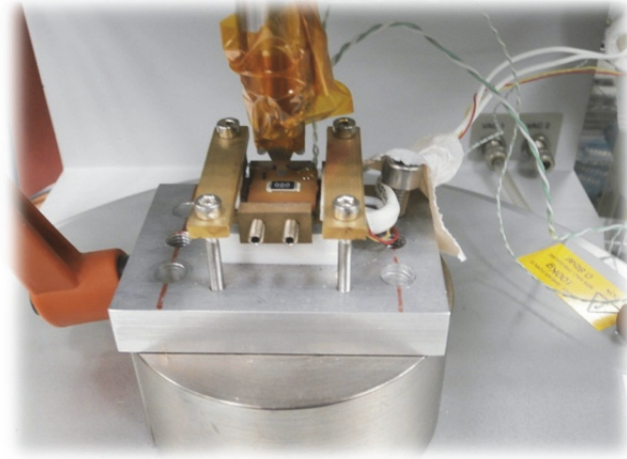


Figure 10: Hot shear test arrangement

4. RESULTS

The resistor assemblies were exposed to three ageing regimes: dry heat, thermal cycling and damp heat. They were dry heat aged at 175 °C, 200 °C, 250 °C, thermally cycled between 20-150 °C, and damp heat aged at 85 °C/85%RH. Shear and resistance measurements were recorded at 0 hours, 190 hours/cycles, 422 hours/cycles and 1137 hours/cycles. Shear results are shown in Figure 11.

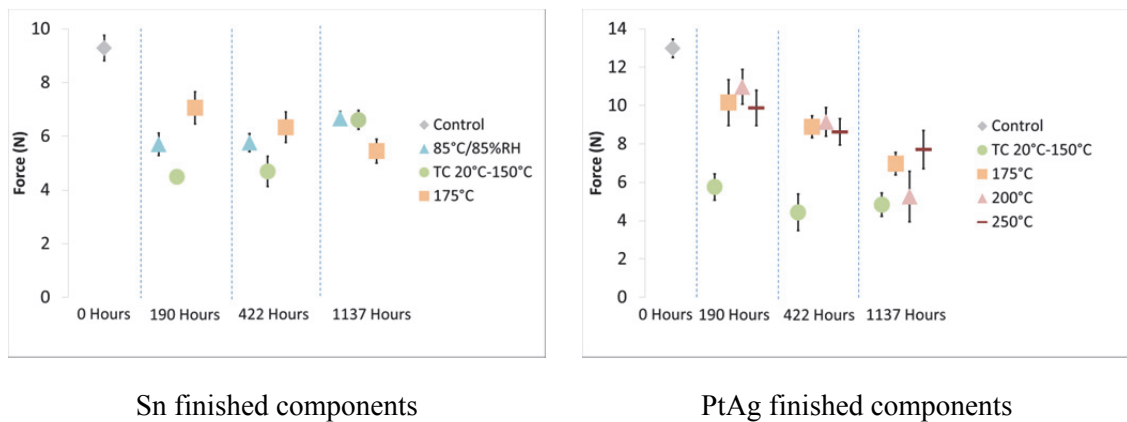
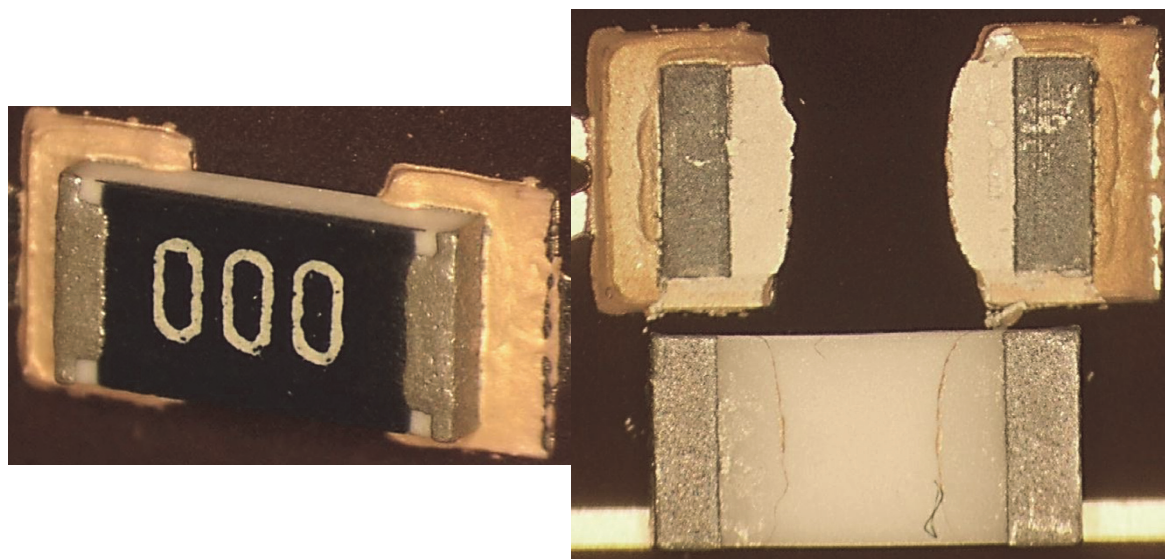


Figure 11: The average shear force for Sn and PtAg finished components. The error bars are the standard deviation.

A typical sample prior to and after fracture is shown in Figure 12. The sample shows brittle fracture with very little or no silver left on the component.



Component prior to fracture

Component and pads after fracture

Figure 12: Samples prior to fracture and after fracture

Higher shear forces were achieved with components with the PtAg finish, over the Sn finish. This could be due to the higher assembly process temperature for the PtAg samples, but is more likely to reflect the solubility and diffusion of the Sn into the sintered silver. Diffusion of the Sn could adversely affect the silver integrity due to the formation of brittle SnAg intermetallics. The isothermal ageing and humidity conditioning only caused a gradual reduction in shear strength, whereas the thermal cycling appeared to have halved the shear strength at the 190 cycle point. This indicates that one of the joints may have been fractured.

Electrical measurements did not show a significant deterioration. Surprisingly, even the thermally cycled components revealed little change. After 1036 cycles, the Sn components resistance had increased from the as manufactured value of 57 mΩ to 230 mΩ. This may be due to the fractured surface, while not mechanically joined, is still in intimate contact and held in position by the other joint.

IPTM results: Increasing amplitude loops were obtained for samples B9 and B10 and are shown in Figure 13 and Figure 14. It is interesting how the higher amplitude loops bend over and the lower amplitude are not contained within them, i.e. there is a rotation of the loops (the same displacement is acquired with a lower load). This might be due to fatigue of the interconnect, or other permanent deformation during these loops. At these high forces the tensile stress is ~60 MPa in the supporting arms, which is the yield strength for silver and hence some ductile behaviour may be expected. However the interconnect between the supporting arms experiences higher shear stresses, and since the shear yield strength of silver (according to the von Misses yield criterion), is ~36MPa, the interconnect should yield in a ductile fashion and dominate the non-elastic behaviour.

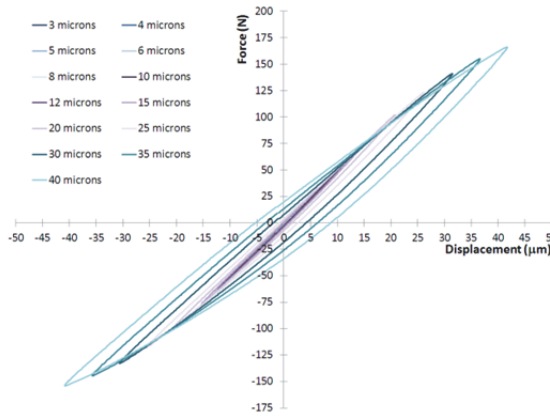


Figure 13: Hysteresis loops for B9 with increasing displacement amplitude

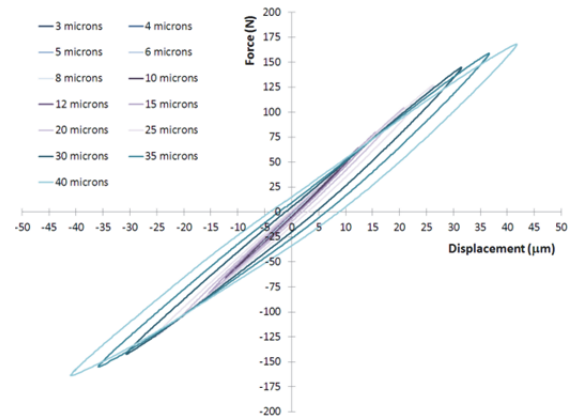


Figure 14: Hysteresis loops for B10 with increasing displacement amplitude

The actual strain, stress and elastic modulus have not been calculated here because of the lengthy calculations and the exploratory nature of the work. Despite this, the curves for the force displacement for increasing hysteresis loops are similar in gradient. This is put down to good repeatability in manufacture. The later samples supported more force; again it is probably due to improved processing, and reflects the infancy of this application and the need for further refinement and process control.

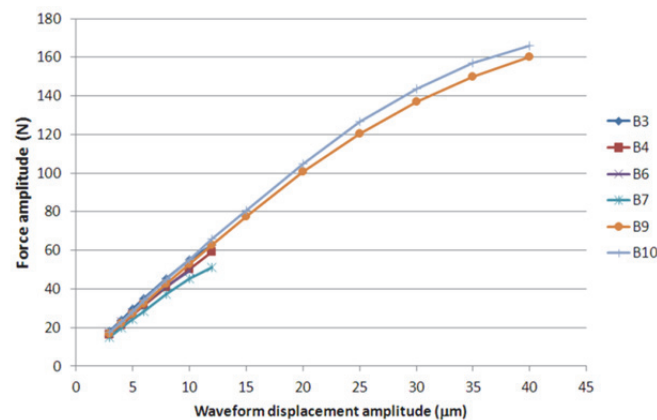


Figure 15: Effect of displacement amplitude on the maximum force for the different amplitude cycles

By plotting the displacement amplitude versus the maximum force amplitude in each cycle, we obtain the response in Figure 15. Only samples B9 and B10 survived to 40 microns displacement. The earlier samples were made with lower process temperatures, as part of the process development. The nonlinear part of the curve for B9 and 10 begins at a shear stress that corresponds to ~ 25 MPa. It is not clear if this is due to ductile behaviour, collapse of pores, or some other incremental damage that is occurring at the interface.

IPTM fatigue measurements: A set of samples were fatigued between 20 and 40 μm displacement range with 200 second dwells and 400 second ramps. Sample B9 was fatigued with a 40 micron amplitude waveform; B10 and B11 were fatigued with 30 micron amplitude waveforms, and B12 and B14 with 20 micron amplitude waveforms. The supported amplitude

vs cycle number for all five samples, are shown in Figure 16. The work done per cycle vs cycle number is shown in Figure 17.

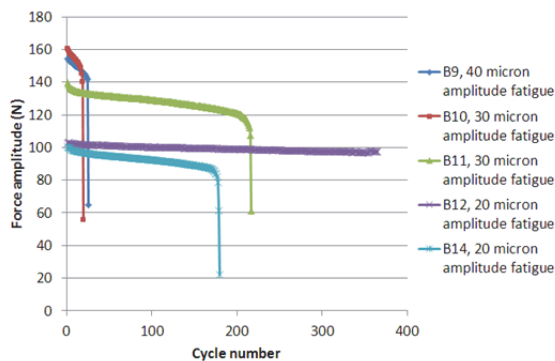


Figure 16: Supported force amplitude versus cycle number

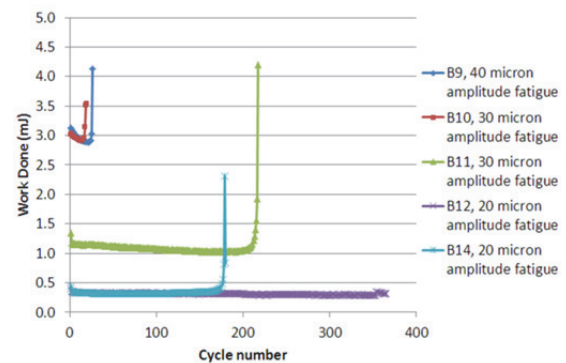


Figure 17: Work done per cycle versus cycle number

The results are similar in showing a gradual drop in the supported force until the last few cycles when it reduces rapidly. The work done per cycle and size of the hysteresis loops change little during the early part of the fatigue process, only decreasing slowly due to the lower supported force. Towards the end, as the hysteresis loops widen, the work done per cycle increases. The number of cycles to failure is shown in Figure 18, and for this limited data set shows approximately linear increase in cycles to failure with displacement range. Clearly, at lower displacement ranges the cycles to failure must increase dramatically, and the relationship is not linear.

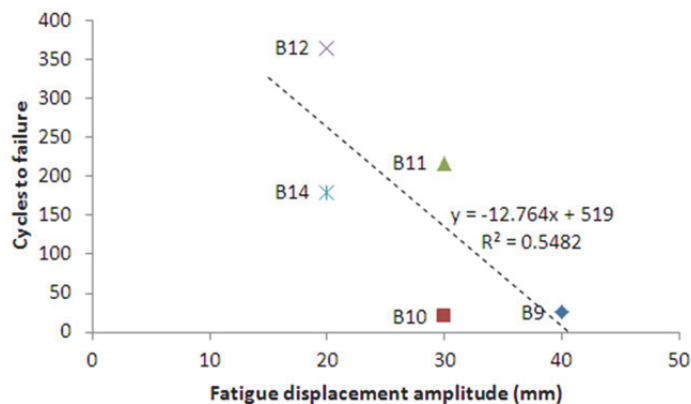


Figure 18: Comparison of cycles to failure between 20 and 40µm amplitude waveforms

Examples of the force and the hysteresis loops are shown in figures 19 to 26 for tested samples.

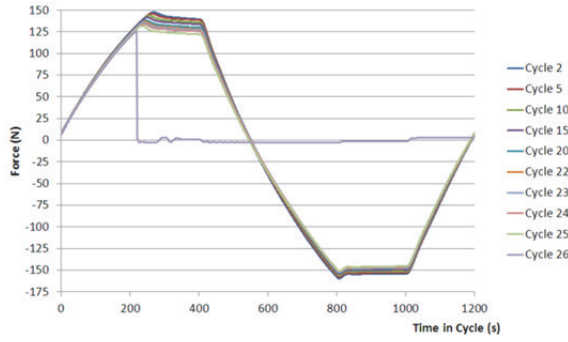


Figure 19: Sample B9. Force Vs time in cycle, with a $\pm 40 \mu\text{m}$ displacement range

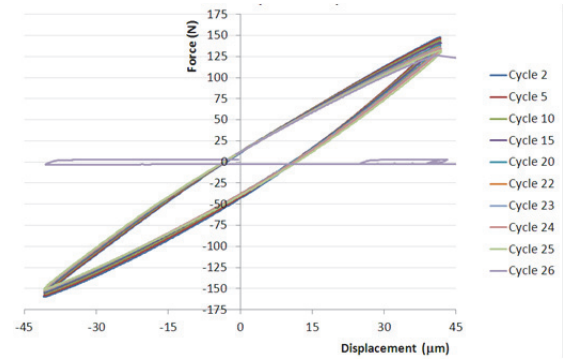


Figure 20: Sample B9. Force Vs Displacement for selected hysteresis loops, with a $\pm 40 \mu\text{m}$ displacement range

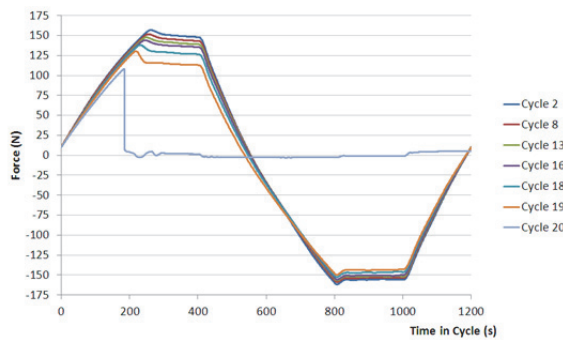


Figure 21: Sample B10. Force Vs time in cycle, with a $\pm 40 \mu\text{m}$ displacement range

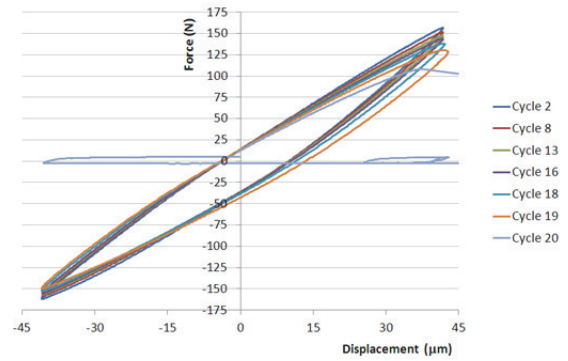


Figure 22: Sample B10. Force Vs Displacement for selected hysteresis loops, with a $\pm 40 \mu\text{m}$ displacement range

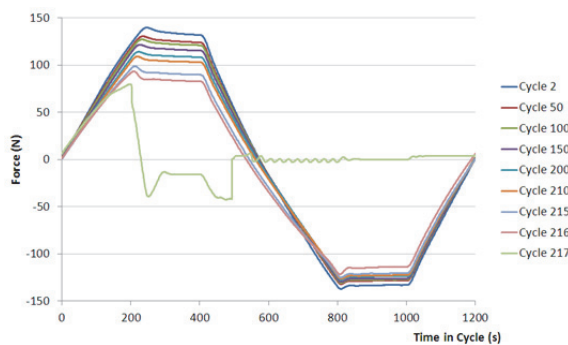


Figure 23: Sample B11. Force Vs time in cycle, with a $\pm 30 \mu\text{m}$ displacement range

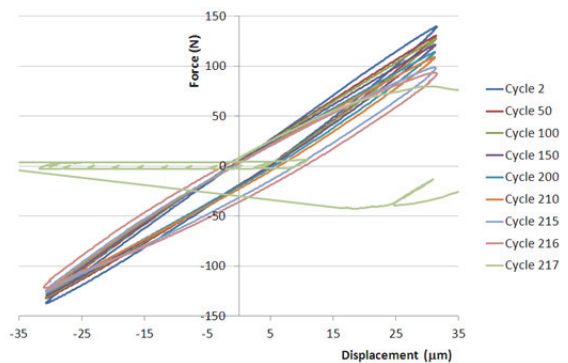


Figure 24: Sample B11. Force Vs Displacement for selected hysteresis loops, with a $\pm 30 \mu\text{m}$ displacement range

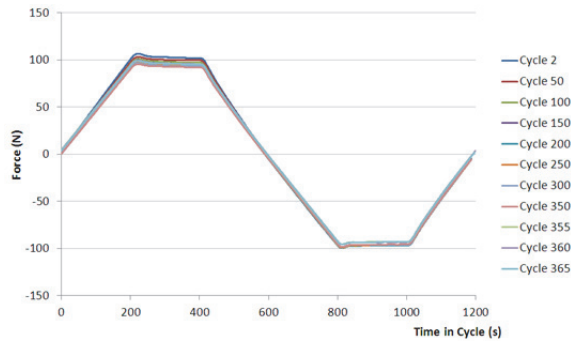


Figure 25: Sample B12. Force Vs time in cycle, with a $\pm 20\mu\text{m}$ displacement range

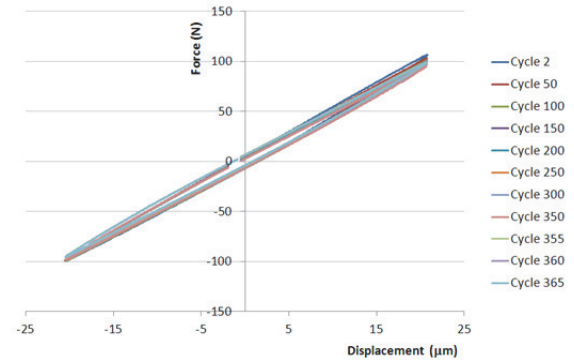


Figure 26: Sample B12. Force Vs Displacement for selected hysteresis loops, with a $\pm 20\mu\text{m}$ displacement range

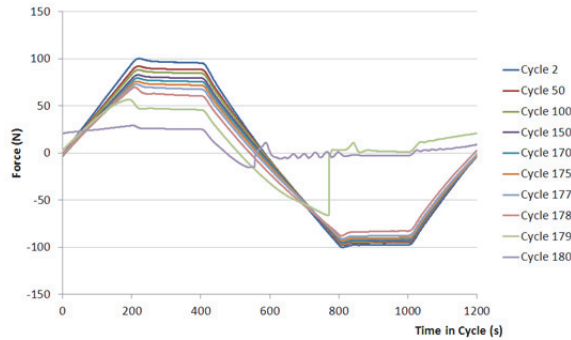


Figure 27: Sample B14. Force Vs time in cycle, with a $\pm 20\mu\text{m}$ displacement range

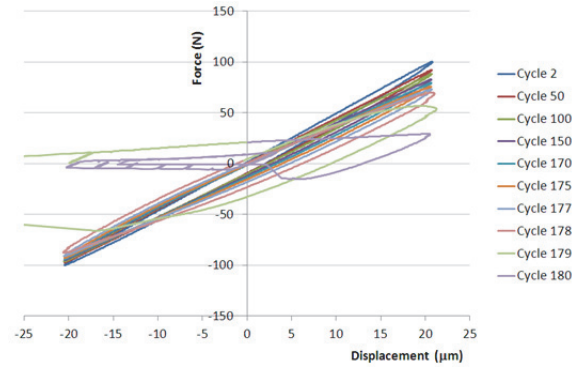


Figure 28: Sample B14. Force Vs Displacement for selected hysteresis loops, with a $\pm 20\mu\text{m}$ displacement range

The fatigue experiments showed a gradual decay in supported force followed by a widening of the loop and increase in work done toward the end of the fatigue, but this trend was not that large when compared to the behaviour of solder.

Sections of the IPTM samples are shown in Figure 29 and show a well formed joint on the left and at a higher mag on the right a sample after fatigue. The fracture occurred interfacially at the top of the sintered joint.

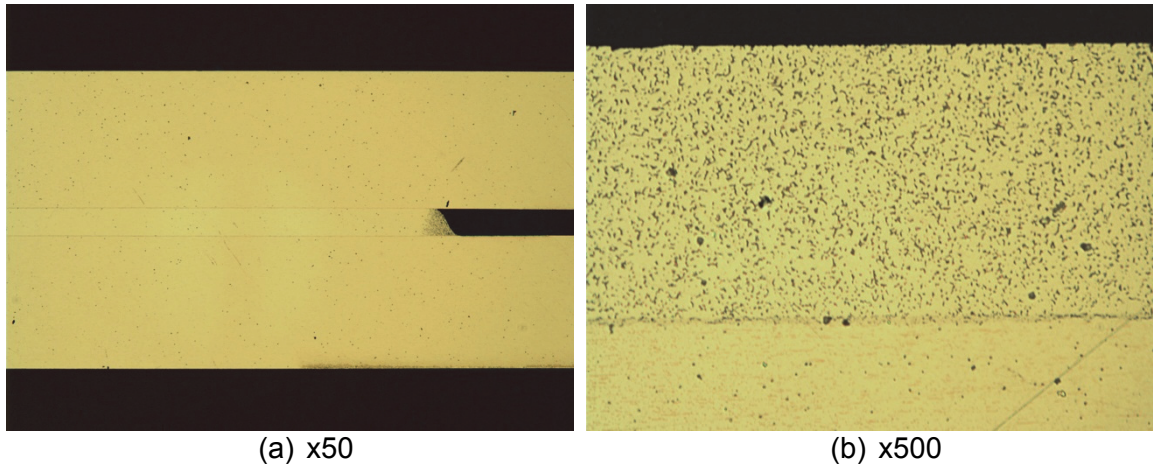


Figure 29: IPTM sintered silver joints. (a) shows the as manufactured joint, and (b) shows the fatigue sample B11, after $\pm 30 \mu\text{m}$ displacement, and reveals the interfacial failure at the top.

Hot shear experiments: The premise for this work was that at higher temperatures we would not see a drop off in the shear force. Hence, the initial measurements were made above 100°C , but low shear forces were observed and therefore further measurements were made below 100°C . The results of these tests are shown in Figure 30. These results show that there is an approximately linear downward trend of shear strength with temperature.

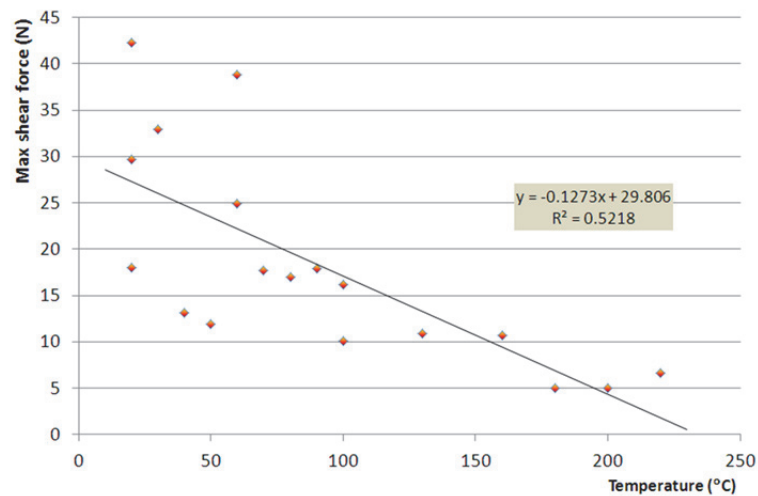


Figure 30: The effect of shear testing at elevated temperatures

Further experiments were performed with the hot shear set up based on using an all silver system. The shear force response is shown in Figure 31.

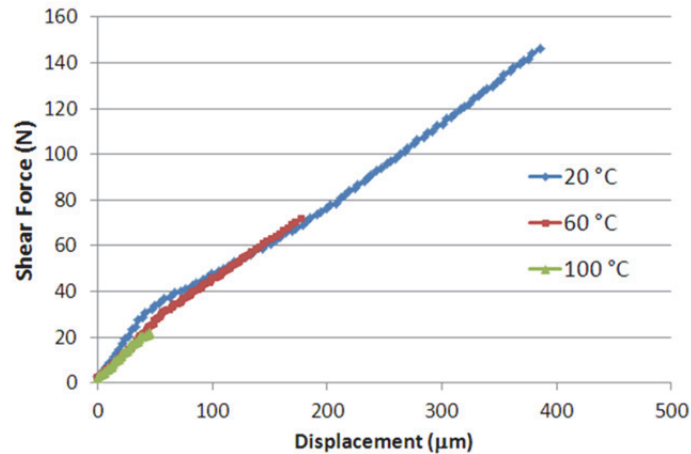


Figure 28: The shear force of sintered silver on silver at three temperatures

These results show the increasing reaction force as the shear tool pushes against the sample, up to the point where the joint fails. Even for these all silver system samples, the failure still occurs at lower forces with increasing temperature.

5. DISCUSSION

The difficulties encountered in developing the assembly parameters indicate that there are critical material compatibility issues, regarding the surface metallisation of the various parts. This outcome reflects the difficulty that will be encountered as alternatives to high lead alloys are rolled out and the need for metrology to characterise performance.

While sufficiently robust attachment was achieved, the authors encountered greater difficulties than expected. Small differences in PCB finish and different batches of components than previous investigations may account for these differences. However a previous assembly process needed to be revisited, and the energy needed to make successful joints increased. This is a current reflection on the immaturity and difficulty of using this technology.

In Annex B, the literature survey, the role of organic components in the paste are discussed. From this it is clear that these need to be removed for successful joining. It is possible that the assembly process used here did not fully remove all the organics, and furthermore there may have been a concentration of these residues at the interface. A further factor is worth noting, in that the IPTM samples were made by printing on both surfaces to be joined, whereas the component assemblies were only printed on the substrate surface. The IPTM samples performed very well and this could be an important observation, and a possible requirement going forward. This observation has been made in the literature, see Annex B. However, a requirement to print sintering paste onto electronic components and baking before assembly would be extremely difficult to encompass.

It is known that using tin finished components is problematic, with the diffusion of tin into the silver creating compositional gradients and potential defects in the interface region. These results showed that lower strength joints were made using the tin finished components, and that these deteriorated at a slightly greater rate.

IPTM results showed little evidence of fatigue, with the hysteresis loops not broadening greatly. Analysing the force time curves, it can be seen there is little evidence of creep, but some relaxation can be seen. However, what is very remarkable is that the 20, 30, and 40 μm displacement corresponds to 15, 27, and 38% shear strain, which includes a correction for

extension in the arms having been applied. A typical high level of shear strain for a solder joint would be 3%, hence although we do not see any fatigue, we are observing an extraordinary high level of compliance in the sintered silver. It would be expected that the application of 3% shear strain to these sintered silver joints that they would outperform solder joints. This is a significant finding. The IPTM data in this report has all been acquired at room temperature, elevating the temperature would yield very valuable data. The IPTM however cannot attain the envisaged operating temperature and a new instrument will be required, for which we have a clear idea of the performance metrics and how that instrument could be realised.

The ageing and shear results revealed that isothermal ageing and humidity only caused a small deterioration in shear strength. The degradation mechanism occurring during this ageing is unknown. The thermal cycling did cause a significant step change and drop in shear strength. This may be occurring because the height of the sintered silver joint is of the order $12\mu\text{m}$, and for this thermal cycle that corresponds to a shear strain of 12%. This is still a very high shear stress, and failure after a few cycles is not unexpected. In the future with improved processing the joint height could be controlled to be $>50\mu\text{m}$, reducing the shear strain to $<3\%$, and hence improving the thermal cycling resistance.

The hot shear results showed that as the temperature was increased the shear strength diminished, and this occurred for the all silver sample as well. This behaviour is unexpected. The sintered silver itself does not appear to be failing; the failure location appears to be interfacial. Furthermore this interfacial strength diminishes rapidly with temperature. This set up was a simple modification of a commercial apparatus, and had limited capability. Further development of a hot stage fixture would allow a wider and more detailed investigation.

In all these studies the failure was not observed to occur within the sintered silver, but at the interface. Clearly this is a weak point in this interconnection technology. Surface preparation is a key factor, and the ability of the sintered silver to bond with the metal termination on the substrate is key. The paste suppliers advise their materials work with silver and copper, and should work well with gold. Since this is a non-wetting joining process, and reliant on inter-diffusion, any diffusion barrier will be problematic. The liquid component in the paste, presented in the literature survey, discusses their properties in terms of promoting self-sintering, the challenge remains for this liquid media to also achieve an action akin to fluxing in soldering. The solubility and thickness of the metallisation on the terminations is therefore critical to adequate bonding. Further work to characterise surface condition and its relationship to future bond strength is needed.

Another consideration for low shear strength at elevated temperatures is that the manufactured sintered silver joint is still not a fully dense solid. Hence, the joint will have a lower melting point, in the same fashion as the nano-silver particles, which is due to the low surface energy. After sintering the resultant structure still has not been fully compacted and there are many unconnected internal pores. This will allow the silver to diffuse easily at elevated temperature. By raising the temperature of the joint, the silver is able to diffuse at lower forces than at room temperature. Extended time at high temperature/higher temperature sintering would be expected then to increase the high temperature strength of the interconnect. This needs to be tested.

The analysis and observations reflect this paste only. It is not clear that the same trend will be seen for other sintered silver pastes/systems. However this joining technology is still in its infancy and further developments by the material manufacturers will undoubtedly improve on the performance observed here.

6. CONCLUSIONS

Mechanical testing has shown that a well prepared joint shows a high level of compliance, and 200 cycles with 27% shear strain can be achieved at room temperature. By comparison solder joint testing is usually undertaken with 3% shear strain.

Ageing of assemblies built with tin and silver finished resistors showed a gradual loss of joint shear strength when tested at room temperature after ageing at temperatures up to 250 °C. Thermal cycling up to 150 °C proved to cause rapid mechanical failure, but the equivalent shear strain was very high at 12%. Electrical performance was largely unaffected.

Hot shear testing showed a rapid loss in strength with increasing temperature. Since failures were interfacial, bonding to the substrate is clearly of critical importance. Furthermore since the manufactured joint is not fully consolidated and contains pores, the joint can be expected to deform increasing easily as the temperature is raised.

This work has shown that fabricating joints that perform well is challenging. The metallisation of the surface being joined needs to be selected and prepared, so that it is compatible with the sintered silver material and process. A silver finish is probably optimal. Printing paste on both surfaces improves the joint quality, as seen with the IPTM samples.

The work has shown that this material does offer a potential solution to the high lead alloys, but there remain challenges. Improved metrology capability is required if these materials are to be fully characterised. Assembled and lifetime assessment techniques are in their infancy.

Suggested metrology developments:

- High temperature mechanical testing with IPTM
- Flexible hot shear tester
- Characterisation of surface condition and impact on joint quality
- Characterisation of sintering process and organic phase emissions and residues

Suggested technology characterisation

- Understanding of various sintered silvers and the assembly process variables: temperature, time and pressure
- Understanding the effect on interfacial adhesion of the metallisation on substrates and components

7. REFERENCES:

1. *Novel Testing Instrument for Lead-Free Solder Characterisation*, D. Di Maio, O. Thomas, M. Dusek, C. Hunt, *IEEE Transactions on Instrumentation and Measurement*, Volume: 60, Issue: 10, Pages: 3444-3450, October 2011

Annex A:

RoHS Issues and Solutions for Level 1 Interconnect Applications

This annex has been compiled by Andy Longford of PandA Europe

Contents

1)	Executive Summary.....	18
2)	Introduction	18
3)	The RoHS Directive Status	19
a)	RoHS Exemptions:	19
b)	Understanding “RoHS-5” and “RoHS 6”	21
4)	Application Demands:.....	22
a)	Power Electronics	22
b)	LED Lighting	22
c)	RF Communications	24
d)	Industrial Applications:.....	24
e)	Automotive Applications:.....	25
f)	Aerospace & Defence (Security) Applications:.....	26
g)	Medical Applications:.....	26
5)	Die Attach Methods	27
a)	Epoxy bonding.....	27
b)	Eutectic bonding	28
c)	Solder Attach	28
6)	New Bonding Options.....	29
a)	Conductive adhesives	30
b)	Reactive Material technology (Nanofoil)	30
c)	Sintering.....	32
d)	Transient Liquid Phase (TLP).....	33
7)	Bonding Process Issues.....	34
a)	Die Attach Voids	34
b)	CTE	35
8)	Replacements for “High-Lead” Solder Materials.....	36
a)	Ag-In materials:	36
b)	Ag-Sn materials:	37
c)	Cu-Sn materials.....	37
d)	“Sintered Silver” epoxies.....	38
i)	Material 1 - NBETech – NanoTach.....	39
ii)	Material 2 – Henkel	41
iii)	Material 3 – Heraeus Materials - “MAGIC” microbond	42
iv)	Material 4 – Cookson “Argomax”	44
v)	Material 5 - DuPont	46
vi)	Material 6 – GEM UK	47
e)	Bismuth/Silver	47
f)	Gold sinter paste	47
9)	Measurement Requirements.....	48
10)	High temperature Solder projects in Consideration:	52
	Appendices.....	53
	Appendix 2 Interconnection Levels:	58
	Appendix 1: RoHS exemptions.....	53

1) Executive Summary

This report covers the work undertaken in the review of the key issues affecting the future needs of level one interconnect (basically die attach) processes that are implicated by the RoHS recast Directive 2011/65/EU which is referred to as RoHS II, or RoHS 2 or RoHS recast.

The report provides a brief, broad based review of the major issues now being presented by the need to change interconnection options to meet the requirements of the RoHS directive. In 2016 the directive exemptions, currently in place, will no longer be allowed. This is already having an impact upon the Power electronics Semiconductor packaging and Printed board Assembly Industry.

There are a number of alternative options to “high-lead” solders being offered. These have been reviewed, with particular emphasis given to the options for Semiconductor “level 1” device interconnection using such lead-free materials and processes. This covers a brief evaluation of the potential lead-free joining technologies and a review of the strengths and weaknesses of these technologies.

This report considers the most likely technology for general high reliability implementation. A considerable amount of ‘in-depth’ material is available for all of the technologies reviewed and this has constituted the source of the information detailed in this report. The most relevant supplementary information has been referenced accordingly, to enable further specific investigation as required. It has considered the aspects of implementation, technology readiness levels and identified areas where additional qualification is required to enable application of relevant technologies. It has also considered what activities need to be in place to support the selection of application suitable technology.

Introduction

“Lead-Free” electronic components and systems have developed over the last 10 years as a result of the European Union (EU) directives for the removal of hazardous substances (RoHS) and other environmental legislation.

The RoHS Directive 2011/65/EU which is referred to as RoHS II or RoHS 2 or RoHS recast, was published in May 2011 for implementation starting October 2012. At that time the directive included the removal of lead (Pb) solders in electronics and indicated that it would apply to all electronic components, device and system manufacturers in Europe after 2014. However a number of exemptions were included (see appendix 1).

In 2016 virtually all of these current exemptions will be removed and full compliance with this directive will be required to what is now widely referred to, by the electronics industry as “RoHS 6”. This descriptor relating to the complete removal of 6 ‘hazardous’ substances which are:

- Lead (Pb)
- Mercury (Hg)
- Cadmium (Cd)
- Hexavalent chromium (Cr6+)
- Polybrominated biphenyls (PBB)
- Polybrominated diphenyl ether (PBDE)

PBB and PBDE are flame retardants used in several plastics. Hexavalent chromium is used in chrome plating, chromate coatings and primers, and in chromic acid.

There are some considerable issues now being raised by this imminent change in the current status of the RoHS “lead-free” directive, which has a range of exemptions and there a number of issues affecting the future needs of level one interconnect (basically die attach see appendix 2) processes that are implicated by the RoHS recast.

In line with the original RoHS directive, component manufacturers as well as PCB manufacturers have virtually changed all processes to lead free compliant EEE parts and PCBs. There are now very few suppliers of PCBs with fused tin/lead able to manufacture components and boards used for space applications. So even though the exemptions for some equipments, such as Aerospace may still apply, it is expected that new qualifications will need to be applied to many components, as from 2014 it will be very unlikely to be able to procure or manufacture any components with leaded finishes.

The need for alternative “die attach” joining technologies is now a very high priority. There is no “drop-in” replacement available for existing ‘high temp’ leaded solder materials that are still being used for power devices and other high temperature components. However, through literature searches and other market knowledge sources it is evident that a number of “possibles” are being developed.

There are many ongoing evaluations being undertaken for all the potential leadfree joining technologies disclosed and an assessment of the strengths and weaknesses of the potential options is reviewed in this report.

The results of the evaluations should eventually offer a set of guidelines and proposals for alternative die attach processes but it is evident that much further full evaluation of each of the possible techniques needs to be completed in order to enable the choice of process most suited to applications for general high reliability joining. The aspects of implementation and technology readiness levels can identify areas where additional qualification is required for many applications and a number of process controls need to be in place to support the selection of relevant application suitable technology.

2) The RoHS Directive Status

a) RoHS Exemptions:

RoHS II exempts certain applications from the substance restrictions. The current list of exemptions is contained in Annex III.

On September 24, 2010, the European Commission adopted a substantially revised list of RoHS exemptions and replaced the entire Annex for clarity. Exemption 39 for cadmium in LEDs is new. Exemptions 1, 2, 3, 4 5, 7, 8, 11 and 25 were broken into subcategories with more specific definitions and conditions of use. Exemptions 9a, 10, 22, 28 and 35 were deleted because they had expired. Adding to the complexity is the fact that printing errors in the Decision are corrected by a Corrigendum, meaning there is no one document that contains the correctly printed new Annex.

September 8, 2011, the European Commission added Exemptions 7(c)-IV and 40 to the Annex.

More than half of the exemptions have expiration dates (many expired in 2011). Some expiration dates are absolute, some allow reduced amounts of the hazardous substance thereafter, and some allow continued use in spare parts.

Specific exemptions for medical devices and monitoring and control instruments are listed in Annex IV of ROHS II.

For a view of the list of exemptions to RoHS, see appendix 1 or refer to:

[Directive 2002/95/EC - RoHS](#)

[Decision 2010/571/EU](#)

[Corrigendum 2010/571/EU](#)

[Decision 2011/534/EU](#)

Exemptions to RoHS are granted to narrowly-defined applications for which the elimination of the prohibited substance is technically or scientifically impracticable or when the only available substitution produces more negative than positive benefits to the environment, health, or consumer safety.

Exemptions are temporary in nature and subject to review at least every four years, until such time as a reliable and safe substitution is available. For this reason, many exemptions carry an expiration date.

Table 1: List of Key exemptions to RoHS Affecting Electronic Component interconnections

Unless otherwise stated, these exemptions will expire on 21 July 2016.

7a	LEAD in high melting temperature type solders (lead-based alloys containing 85 % by weight or more lead)
7b	LEAD in solders for servers, storage and storage array systems, network infrastructure equipment for switching, signalling, transmission, and network management for telecommunications
7c-I	Electrical and electronic components containing LEAD in a glass or ceramic other than dielectric ceramic in capacitors (piezoelectronic devices) or in a glass or ceramic matrix compound
7c-II	LEAD in dielectric ceramic in capacitors for a rated voltage of 125 V AC or 250 V DC or higher
7c-III	LEAD in dielectric ceramic in capacitors for a rated voltage of less than 125 V AC or 250 V DC. <i>Expires on January 1, 2013</i> (except spare parts for EEE placed on market before Jan 1, 2013)
7c-IV	LEAD in PZT-based dielectric ceramic materials for capacitors being part of integrated circuits or discrete semiconductor
14	LEAD in solders consisting of more than two elements for the connection between pins and package of microprocessors with lead content of more than 80% and less than 85% by weight. <i>Expired January 1, 2011</i> (except spare parts for EEE placed on market before Jan 1, 2011)
15	LEAD in solders to complete a viable electrical connection between semiconductor die and carrier within integrated circuit flip chip packages
33	LEAD in solders for the soldering of thin copper wires of 100 µm diameter and less in power transformers

b) Understanding “RoHS-5” and “RoHS 6”

RoHS-6 is a term that is now being used by the Semiconductor Electronics industry. Derived by the PCB industry, in the USA and Asia, RoHS-6 generally means that the “product” does not contain any RoHS restricted material. For companies that are exempt (- until July 2016) from the Pb restrictions (section 7), they can use products that are termed as “RoHS-5”.

Common component and systems classifications are:

- RoHS 6 (6/6): This implies that the Component PCB meets the above limits
- RoHS 5 (5/6): The PCB meets the above limits except that it exceeds the lead limit & customer is taking lead exemption

According to Indium RoHS-5 may not be a legal definition but it is a term that is commonly used in the industry because there are multiple aspects of RoHS compliance.

Only the company with its name on the final electronic product can declare something RoHS compliant.

The term doesn't actually apply to parts or consumables because only the supplier of the finished product can determine compliance as the term "compliance" varies based on the type of product being sold. For example, a military electronics device is "RoHS compliant" even though it contains Pb based solders. Since Pb is really the only restricted item that has a large number of exemptions. The term RoHS-5 was coined to indicate that this assembly needs to comply with the EU regulations but the end product is considered exempt from the Pb restriction.

RoHS-5 is simply to say that your product is RoHS compliant with clause 7b and, for semiconductor devices, clause 15 exemptions.

PCB's having SnPb solder plating can qualify for this exemption when other RoHS restricted substances are not present in it.

RoHS-6 Products are compliant for all Six restricted substances

This is the most commonly implemented form of the Directive. RoHS-6 products do not have any of the six banned substances (Lead, Mercury, Cadmium, Hexavalent Chromium, PBB, or PBDE) in amounts exceeding the allowable maximum concentrations defined in the Directive. The Directive delineates these concentrations as the percent of the weight of any individual homogeneous component used within the equipment; not as a percentage of the aggregated weight of all components in an assembled product.

The RoHS Directive allows exemptions when adequate substitutes cannot be found. Exemptions relevant to power conversion products include:

- Cadmium plating used on relay contacts
- Lead usage in some alloys
- Lead used in ceramic capacitors

Note that exercising any of the lead exemptions listed above does not alleviate the need to use lead-free solder, including PCB solder finishes. Many companies list any exemptions that were taken on the RoHS Certificates of Compliance in order to document adherence to the Directive.

3) Application Demands:

a) Power Electronics

Power Electronics is vital to the UK economy and its international competitiveness. Globally, the sector is worth £135 billion, and the UK has a leading position in this market. Overall UK contributes around 3% of the global Power Electronics product (as opposed to component) manufacturing (based on power semiconductor module sales), with a very high percentage of that production being exported.

The new generation Power Semiconductor devices, such as IGBT's, Switches and Converter chips being developed, are utilising Silicon, Silicon Carbide (SiC) and GaN technologies. The development of these emerging technologies is being driven by applications in Energy, Transport, Communications and Control systems, such as Solar power, electric vehicles and the Smart Grid.

However current and emerging power devices have issues with thermal management, current carrying capability, and interconnection methods that have demanded high temperature joining processes such as High Lead solders for both die to package interconnections as well as package to board connections.

The new developments need to address a number of more fundamental packaging issues that are pushing the package boundaries.

To ensure that these new devices meet the need to be “smaller, faster, cheaper” as driven by the emerging applications in switch mode power supplies (SMPS), motor control, energy conversion and health management systems, the packaging processes are having to adopt novel advanced packaging features, developed primarily for the generic high speed digital Semiconductor ‘chip’ industry. These include TSV, solder ball array and 3D chip packaging.

The power device package performance is a significant factor and has an important role in solving system requirement challenges. The package is required to protect the chip from environmental influences, enable testing and utilise standard processes to mount it onto the PCB. It is also a means of providing improved lifetime and reliability by enabling additional thermal management, current carrying capability and high voltage isolation.

The change from High lead solder to Lead free in order to meet the demands of “RoHS 6” poses some major problems:

- The emergence of replacement joining materials is still “in development”.
- The timescales to meet the removal of the RoHS exemptions section 7 and 15 by July 2016, means that qualification of new systems should have begun at the start of 2014.

b) LED Lighting

LED lighting provides many advantages in terms of efficiency, longevity and maintenance costs. LED lighting is now main stream – and although the technology is still developing, since introduced in the 1970's, it is believed that the LED revolution is over. Predictions are that LED will be the dominant lighting technology by 2020.

The LED lighting market is forecast to grow by 45% per year until 2019 and go from a value of \$4.8bn in 2012 to \$42bn in 2019, according to a WinterGreen Research report. The report listed ten market leaders in the industry. These are Philips, GE Lighting Solutions, Maxion Technologies, QD Vision, Lighting Science Group, Osram, Toshiba, Solid State Lighting Systems, Mitsubishi / Verbatim and Cree.

In 2011, the UK LED lighting market was estimated to be worth around £105 million at manufacturers' selling prices (MSP) and is dominated by sales of luminaires, which accounted for 90% of the market, with replacement lamps accounting for a further 8% and lighting controls the remaining 2%. Many current LED luminaires and modules are integrated. These products are not easily replaced as they require mechanical fasteners to couple the LED to the heat sink. This is changing as more replacement lamps and modules are being brought onto the market but means the traditional product split is becoming more difficult to define.

MTW Research have published Research & Analysis market report of the UK Lamps & Luminaires Lighting Market in 2013 with forecasts to 2017. It is based on industry data from more than 360 lighting suppliers active in the UK lighting market and includes the UK LED Lighting Market 2007-2013 with forecasts to 2017.

LED lighting generally complies with RoHS regulations as it does not contain mercury but Leaded solders (high temperature) are still used in some die attach processes for the LED element. Most lighting suppliers can assure that all the materials, with the exception of the LEDs, are recyclable, so LED lighting tends to eliminate the disposal concerns associated with fluorescent tubes, which are subject to environmental legislation.

These new LED technologies require new standards and testing benchmarks. Buyers want to be able to confidently purchase a solution that works well and manufacturers need to know devices are compliant. Industry regulation is desperately needed. The lighting needs a standard or kite mark that proves that product has been independently tested and qualified. But until there is a formal industry standard then buyers must ask the supplier for all relevant documentation.

NPL's LED group are working with UK companies to set "quality" standards, see:

<http://www.npl.co.uk/upload/pdf/led-lighting-spec-2012.pdf>

This is the fourth edition of the guidance notes produced under the umbrella of the Lighting Liaison Group, which is an informal group representing the major lighting organisations in the UK. This guideline indicates the quality criteria from the IEC/PAS documents and users of LED luminaires should always ask for LED luminaire specifications measured in compliance with these new IEC/PAS documents.

The benefits of LED technology are completely dependent upon longevity in the fitting. And longevity in a LED light engine is completely dependent upon three crucial factors:

- The LED itself
- Thermal management of the junction temperature
- The driver

Responsible LED lighting suppliers will have independent test data for each of those factors as well as photometric data, CE marking and IP rating certification, TM 21 reports and LM 80 reliability data. They will also be happy to share case studies and provide reference sites to visit.

There is a huge gulf in the quality of different LED lighting solutions. From an industry perspective, standards and regulations should provide a platform for consistent language in regard to definitions, test methods, laboratory accreditation and for product design, manufacturing and testing.

It should be noted that compliance with RoHS is assumed by most users of LED light engines, as it is expected that RoHS is the first "standard" or compliance factor that should be applied. Most LED lighting will use High Brightness (HB) or High Power LED elements. Of these many use

high lead solders for the die attach. The manufacturing of the LED parts will now need to be regulated. The requirements are therefore similar to those of the power electronics market covered in section 4a above but qualification timescales are not as stringent to the extent of LED element 'qualification' being non-existent in terms of RoHS.

In December 2013, the WEEE regulations 2013 were laid before UK parliament. As expected, they contain some important changes in that LED light sources (which include LED lamps and LED luminaires) are put in the same category as gas discharge lamps. This will avoid the risk of an orphan waste stream as gas discharge lamps are replaced by LED lamps, and increasingly by LED luminaires.

c) RF Communications

The global communications application market was worth \$446 billion in 2012. Wireless electronics constitutes 75% of the overall market, or \$336 billion spent on wireless phones, infrastructure, and other devices. By 2018, Databeans predicts the overall communications electronics market will be well over \$800 billion with a compound annual growth rate of 11% over the next five years. RF circuits continue to play an increasing role in the overall semiconductor market, covering wired and wireless transceivers, power amplifiers, and other RF devices and AFEs.

RF power amplifiers which are integral parts of all base stations for cellular and mobile wireless infrastructure, have a current market size of around US\$ 4bn. They represent one of the most expensive component sub-assemblies in modern wireless infrastructure equipment and both their performance and cost are important drivers in base station design. Efficiency, physical size, linearity, and **reliability** are among the principal concerns. As price pressures become fiercer, new and innovative techniques and materials must be used to reduce the cost of this important component part while still maintaining performance. The RF power semiconductors used in these power amplifiers are the linchpin for their cost and capability and they also have keep pace with both the economic and technical realities facing designers and users of these RF power amplifiers, including compliance with RoHS, as per section (a) above.

Thermal performance is key to the efficiency of devices. Much of the packaging is expensive metal / ceramic hermetic seal, so the market is pushing to reduce costs, reduce package costs and find new materials (such as GaN) to reduce sizes as well. Current practice in RF packaging is for Eutectic die attach processes, such as Gold/Silicon or Gold/Tin. High Lead solders are also being used. Replacement lower cost Silver Sinter and epoxies are being tried out to gain lower sizes packages and lower cost assemblies.

d) Industrial Applications:

Most "non-consumer" electronic products can be classified for use in industrial applications where reliability and lifetime outweigh cost requirements. Typical industrial applications are:

- Industrial power converters for controls etc
- Industrial drives for system control
- ASDs (adjustable speed drives)
- Control engineering applications,
- Machine tool applications
- Electronics in power systems, power quality monitoring/control
- DC/DC converters, rectifiers, inverters, matrix converters
- Multi-phase machines and converters
- Pulse width modulation (PWM), multilevel/resonant converters
- Induction, synchronous, permanent magnet motor drives

- Switched reluctance motor and synchronous reluctance motor drives
- Renewable energy, photovoltaics, hybrid systems
- Programmable and computer based controllers, digital control, FPGA
- FACTS devices, active power line conditioners, distributed generation

Key requirements for interconnections in such applications are; need to maintain long term reliability, use in relatively harsh environments, potentially extremes of temperature over lifetimes and potential inclement environments involving dust, dirt, liquids and mechanical vibrations.

The demands on the joining materials for the interconnections have generally been met by use of solders, which provide a level of compliance and offer a good conductive medium. Tin-Lead solder replacement has had a number of concerns but most applications have been successfully supported by the development of SAC alloy solders and conductive epoxies for both die attach and package board interconnections.

e) Automotive Applications:

Mainly applications in the ‘automotive’ market involve the use of electronic components in:

- Electric vehicles, power convertors, regulators and switching controls etc
- Underhood electronics
- Sensors and systems
- Computer control
- “infosystems”
- Engine management

The major differences between automotive electronics and the rest of the electronic industry are; use in a harsh environment, higher and lower temperatures cycled, vibration levels and corrosive/dust environments. In addition, no device redundancy is allowed and lowest possible cost is mandatory.

(See presentation: www.seas.ucla.edu/ethinfilm/Pb-freeWorkshop/abs/pan.html)

The automotive industry continues to push for higher performance interconnections. To increase robustness, there has been a move to use “press-fit” connection technology which is considered more ‘robust’ than solders, for a number of the more challenging and aggressive applications.

High lead solders have been a solution for many of the power modules and power control devices both for board mounting and for especially for die attach within power component packages.

Qualification of new solutions to meet RoHS 6 can take from 6 months minimum up to a possible 5 year process.

The SAE (Automotive engineering institute) has published SAE J1879 – revision dated 21-02-2014, Handbook for Robustness Validation of Semiconductor Devices in Automotive Applications.

The Robustness Validation qualification practices defined in this document do not eliminate the need for qualification procedures found in JEDEC or AEC documents. Rather, these practices integrate robustness design methods (e.g., test to-failure in lieu of test-to-pass) into the automotive electronics design and development process. The document primarily deals with integrated circuit issues, but can easily be adapted for use in discrete or passive component qualification with the generation of a list of failure mechanisms relevant to those devices. Component qualification is the main scope of this document.

f) Aerospace & Defence (Security) Applications:

Most applications in this market still necessitate the use of lead bearing solders as exemptions to RoHS cover requirements. However the need to use more cost effective and ‘available’ technologies means adoption of “lead-free”. This is a longer term process of qualification than other markets.

It is likely that some High Lead solders will remain in use in order to enable spare parts and longevity of existing electronic systems.

Electronic components for defence applications have generally followed process needs laid down by “MIL” standards in particular;

MIL-STD-750 - Test Methods For Semiconductor Devices.

MIL-STD-883 – Test Method Standard Microcircuits.

It is UK government policy to encourage the use of standards that are used worldwide whenever possible. However, when no suitable national or international standard exists that fits a specific need, MOD UK will create a new standard.

g) Medical Applications:

According to market research firm Databeans, total market revenue will grow from \$6 billion to \$10 billion by 2016, with unit shipment increasing from 6 billion to 10 billion units in the same time period. This reflects the demand for medical electronic devices using “medical” semiconductors. For the most part, the growth will be in FDA Class 2, and to a lesser extent, Class 3 products. Class 2 products are bench-top, portable and wearable devices that are not invasive, while Class 3 devices are implantable units such as defibrillators.

A variety of devices are already available to monitor the condition of a person who wants to stay healthy and live independently. They include digital thermometers, pulse oximeters, pulse/blood pressure monitors, weight scales, glucose meters, cardio exercise machines, electrocardiogram devices and insulin pumps. Additionally, there are medical devices used in clinical applications such as ultrasound and scanning devices, digital stethoscopes, MRI and digital X-ray.

The huge advances in medical devices, especially the new mobile and connected devices, are being driven by the latest developments in semiconductors. These include large scale integration and reduced power consumption, but also semiconductor devices specifically targeted at medical applications.

Another important segment in medical electronic device design is that of sensors. Most people know wide area network (WAN) or local area network (LAN). Now a new term called BAN is emerging. It is the body area network in which the body acts as a network to connect to a medical device.

In medical product design, features and power requirements are the key factors in selecting semiconductor devices. Additionally, life cycle management and supply chain management are important, as medical products do not change as fast as consumer products and require long-term vendor support.

The medical market demands are increasing needs for devices with higher speeds, higher precision and lower power in order to enable better performance, smaller equipment, while maintaining the high standards for quality and reliability.

A wide range of standards are applied to medical electronics, depending upon application requirements etc. For example, medical devices should be certified according to the third edition of IEC 60601-1 (Medical electrical equipment - Part 1: General requirements for basic safety and essential performance) and these must be developed under a process compliant with ISO 14971(a risk management assessment standard).

4) Die Attach Methods

Die attach (die bonding) is the assembly step during which a die is mounted and fixed to the package or support structure (header, leadframe, PCB, substrate etc). For high-powered applications, the die is usually eutectic bonded onto the package, using e.g. gold-tin or gold-silicon solder (for good heat conduction). For low-cost, low-powered applications, the die is often glued directly onto a substrate (such as a printed wiring board) using an epoxy adhesive process.

A number of lower cost applications require both good heat dissipation and conductive die attach processes. Many of these have used, and continue to use, a high temperature (high lead) Solder for Die Attach – or similar Level 1/2 assembly – to provide a good thermal path and a conductive bond between die and substrate. These solders have allowed devices to be “reflowed” in heated ambient during PCB assembly processes. The packages or modules heat up externally whilst the solder maintains a good adhesion of the die to the substrate and does not melt or deform.

The Die Bonding process starts with picking the target die from wafer or wafer tray, the most common method is to push the target die from the tape or the tape can also be drawn away from the die by vacuum. The released die is generally picked by a vacuum tool and aligned to a target pad on the carrier or substrate, and then permanently attached, using one of several die bonding techniques.

The key points for good die bonding are:

- The bond material requires a good thermal conductivity to dissipate the heat generated from the die.
- There should be perfect contact required between the chip and substrate without any voids.
- The bond should be made very carefully, so it doesn't destroy the die/chip.
- The bond should stand extreme temperatures without any degradation.

The choice of die bonding process depends upon package sealing strategy, operating conditions and environmental and reliability requirements. The die bonding can be generally accomplished by distinct types of attachments.

a) Epoxy bonding

An epoxy bond is formed by attaching the die to the substrate with the use of epoxy glue. A drop of epoxy is dispensed on the package and the die placed on top of it. The package needs to be heated at an elevated temperature to cure the epoxy properly. This process uses adhesives such as polyimide, epoxy and silver-filled glass as die attach material to mount the die on the die pad. The mass of epoxy climbing the edges of the die is known as the die attach fillet. Excess of die attach fillet results in the die attach contamination of the die surface and little amount used may result in die lifting / tilting or die cracking.

Epoxy adhesives are electrical insulators and have poor thermal conductivity. To improve the electrical conductivity, epoxy or polyimides are filled with the gold and silver material. In order to achieve a lower value of thermal resistance ceramic particles like SiC (Silicon carbide, compound of silicon and carbon) and BeO (Beryllium oxide, an inorganic compound) can be added. Epoxy bonding is mainly preferred due to:

- Low curing temperature
- Can be used for wide range of die sizes

- Can be reworked easily.
- Lower cost

b) Eutectic bonding

Is a die bonding technique with an intermediate metal layer (Au/Al) that can produce a eutectic system. A eutectic system is a mixture of chemical compounds or elements that has a single chemical composition that solidifies at a lower temperature than any other composition made up of the same ingredients. The fact that the eutectic temperature can be much lower than the melting temperature of the two or more pure elements can be important in eutectic bonding.

The most important parameters for eutectic bonding are:

- bonding temperature
- bonding duration
- tool pressure

A eutectic bond is formed by melting a preform consisting of a mixture or alloy of two or more dissimilar metals in the joint between the die and substrate. A typical example is a preform composed of gold and silicon. The melting point of gold is 1640°C, and silicon is 1414°C. However, when the preform is made up from the materials which are the combination of these two, the melting point becomes much lower than the actual melting point of the materials (see table 1). For this method a layer of gold metal has to be pre-deposited on the backside of the die. By heating the package above the eutectic temperature and then placing the die onto the preform (with a scrubbing action), a bond is formed between the die and package substrate.

Table 1. Compositions and Melting Points of some Eutectic Die Attach Preforms

Composition	Temperature (deg C)	
	Liquidus	Solidus
80% Au, 20% Sn	280	280
92.5% Pb, 2.5% Ag, 5% In	300	-
97.5% Pb, 1.5% Ag, 1% Sn	309	309
95% Pb, 5% Sn	314	310
88% Au, 12% Ge	356	356
98% Au, 2% Si	800	370
100% Au	1063	1063

AuSn is brittle, which makes it difficult to produce and process. Due to low ductility and high mechanical strength, AuSn die-attach layers tend to transmit thermo-mechanical stress to the die.

As most Eutectic solders are Au-based, they are therefore relatively expensive materials to use.

c) Solder Attach

Solder attach is a preferred type of die bonding because of the better thermal conductivity of the solder material. Where there is extreme variation of temperature on die during its operation eg a power device, LED etc, solder attach is used as the important concept to dissipate heat generated from the device efficiently. Solder attach generally is referred as soft-solder attach. Soft soldering materials are the low melting binaries and ternaries metallic compositions.

The following steps were involved for solder attach technique:

1. Some initial solder alloy to be pre-plated over the die metallization and the substrate metallization.
2. The components are fluxed, placed together and reflowed.
3. Flux must be cleaned by cleaning mechanism before the device is encapsulated
4. In a fluxless solder wire process, a wire is fed into in-line system where it contacts the pre-heated lead frame which melts the solder and then the solder is formed in desired shape.

Solder attach provides good mechanical strength, high thermal conductivity and good electrical conductivity.

Using High Lead solder:

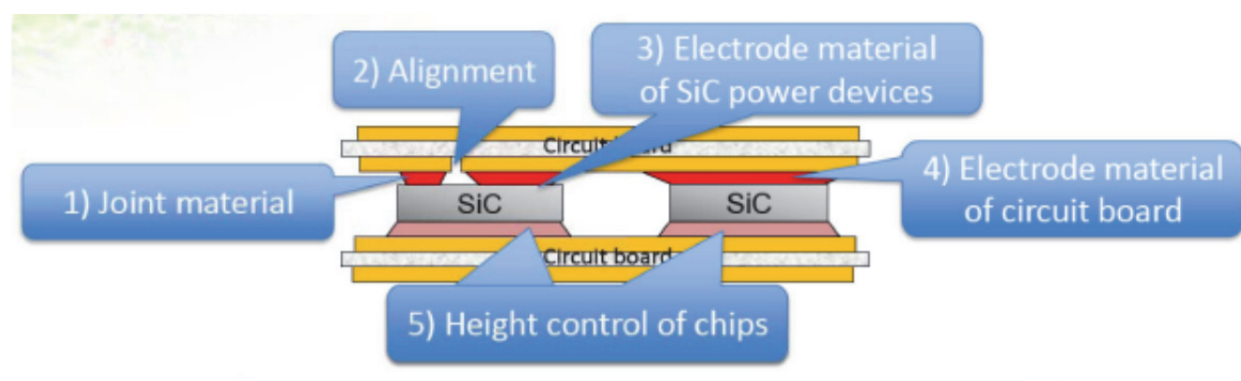
The die-attach layer has two main functions: mechanical fixation of the die on its substrate, and dissipation of heat generated in the die. Especially in power and high-power applications, generated heat density is high. Therefore, conventional die-attach adhesives or eutectic solder alloys are not suitable as die-attach materials.

For these applications, high-melting solder alloys are used, which contain more than 85% lead by weight, and do not satisfy the requirements of RoHS. Since there is no established lead-free substitute on the market, high-lead alloys are included on the exemption list of RoHS for these applications. However, die-attach materials that satisfy the requirements of RoHS do exist. (see following sections).

5) New Bonding Options

Electronics systems are increasingly being applied for monitoring & control in high temperature harsh environments and therefore robust interconnection processes are being required that meet or exceed the performance of the high lead solders.

The diagram below indicates the typical areas that need to be considered in the Die attach process. SiC materials are used in this example, but the same issues apply for GaAs, GAN and LED chips as well as Silicon IGBT devices.



Reference: *National Institute of Advanced Industrial Science and Technology (AIST)* –

	Processing temperature	Max. use temperature	Electrical conductivity $10^5 (\Omega\text{-cm})^{-1}$	Thermal conductivity (W/K-cm)	Die-shear Strength (MPa)	Price (\$/gm)
Lead-tin solder	217°C	< 183°C	0.69	0.51	35	< 1.0
Lead-free solder	260°C	< 225°C	0.75	0.70	35	< 1.0
Gold-tin solder	310°C	< 280°C	0.625	0.58	30 - 60	50 - 80
Silver epoxy	100 - 200°C	< 200°C	0.1	0.1	10 - 40	2 - 9
Sintered nano-Ag	< 260°C	< 961°C*	3.8	2.4	20 - 40	competitive

Above table indicates process temps vs usage temps and relative costs ... Table is from CPES (Georgia Tech).

a) Conductive adhesives

The UMICORE “MICROBOND Gecko” is an adhesive filled with copper, which is currently in test phase at assembly companies. It can be processed like conventional high-lead solder pastes via dispensing or printing, followed by thermal curing, making it a drop-in replacement for solder paste.

Unlike solder paste, no cleaning is required after curing. The adhesive layer shows a composite structure, composed of copper powder particles, homogeneously distributed in a polymer matrix. In comparison to joints made of solder pastes, the adhesive paste exhibits:

- a void rate near zero, rather than 5%;
- high adhesion on conventional part metallizations (copper, nickel, gold, silver, bare silicon);
- high mechanical strength;
- high interface quality to chip and substrate.

With solder paste, the interface between solder and die or substrate is made of an intermetallic compound, which is actually a barrier for heat dissipation. With the adhesive joint, no intermetallic compounds are formed; positively influencing heat dissipation through the joint. These advantages compensate inherent weaknesses of the adhesive like low bulk thermal conductivity, or poorer deformation capability, leading to similar heat dissipation through the adhesive die-attach joint and through a solder joint. Therefore, high thermal fatigue resistance and high package reliability is achievable. This product shows promise as a substitute for high-lead solders in power and high-power packages.

b) Reactive Material technology (Nanofoil)

Reactive materials are similar to insensitive high explosives, but are usually thermite-like pyrotechnic compositions of two or more nonexplosive solid materials, which stay inert and do

not react with each other until subjected to a sufficiently strong mechanical, electrical or laser stimulus, after which they undergo fast burning or explosion with release of high amount of chemical energy in addition to their kinetic energy.

Indium Corporation have developed a product NanoFoil® (NF). - a trademark name of Reactive NanoTechnologies. The Indium – proprietary NanoBond® is the process of bonding materials using NF which is the heat source material used to make the bond.

NanoFoil is a reactive multi-layer foil material, sometimes referred to as a pyrotechnic initiator of two mutually reactive metals, aluminium and nickel, sputtered to form thin layers to create a laminated foil. On initiation by a heat pulse, delivered by a bridge wire, a laser pulse, an electric spark, a flame, or by other means, the aluminium and nickel undergo self-sustaining exothermic reaction, producing an intermetallic compound nickel aluminide (NiAl). The reaction occurs in solid and liquid phase only, without releasing any gas.

Such multilayer materials, whether nickel-aluminium, aluminium-titanium, or titanium-amorphous silicon, are used for joining materials by reactive bonding.

The foil is made in a range of thicknesses, e.g. 60, 80, 100, and 150 micrometers. The flame front propagation rate ranges generally between 7.5–9 m/s. The reaction temperature can reach up to 1500 °C for a millisecond. The velocity and temperature of the reaction can be controlled by adjusting the thickness of the layers. Typical thickness is 50 nm per a bilayer. The thin layers maximize the contact between the metal and lower the activation energy for the reaction, normally too high to allow reaction between bulk aluminium and bulk nickel. The layers are deposited by sequential sputtering of alternately nickel and aluminium.

Nanofoil will ignite on heating to at least 250 °C in rate of at least 200 °C/min. Slower heating will anneal the material, causing loss of its pyrotechnic properties. For electrical initiation, a momentary contact at 10A/5V is sufficient; for ohmic contact, 120-150 amperes is needed for a 15 micrometer diameter contact, and 250-300 A for a 300 micrometer contact.

Nanofoil can be both cut and ignited by a laser. The pulse width and power determines if the material will be cut or initiated.

Nanofoil is frequently used for soldering and brazing, as a heat source. When sandwiched between the components to be joined, either with a foil of solder on each side, using solder precoated components, or using solder-coated NanoFoil, it uniformly delivers significant amount of heat energy across the entire area, melting the solder and only locally heating the surface of the substrates, lowering the heat load on the component in comparison with soldering/brazing in a furnace. An externally applied even pressure during reaction and cooling serves to ensure a good homogeneous joint without voids. This process is known as NanoBond.

Significantly dissimilar materials can be bonded without cracking: semiconductors, metals, ceramics, and polymers. The energy is deposited very locally, without significant heating of the bulk of the substrates, which reduces problems with mismatched thermal expansion coefficients between the materials and allows their joining at room temperature.

As a sacrificial heat source in soldering and brazing applications, NanoFoil® is ideal for high-temperature applications. NanoFoil® becomes a non-functional part of the solder or braze joint, eliminating the need for an oven or furnace and allowing for the use of higher temperature solders.

Microelectronics Applications are:

- RF Power Attach
- Die Attach

- LED Attach
- Packaged Part Attach
- Medical devices
- CPV Receiver Attach

For full application and process details see:

1) Wikipedia

2) Indium Corporation presentation, NanoFoil® - a Localized Heat Source for Precision Bonding by Jacques Matteau, Global Sales Manager. 2010 publication.

3) <http://www.indium.com/nanofoil/#ixzz1ZnhfKaAB>

4) Nanofoil user guide, www.indium.com/_dynamo/download.php?docid=932

c) Sintering

Sintering (wikipedia) is a method for making objects from powder, by heating the material in a sintering furnace below its melting point (solid state sintering) until its particles adhere to each other. Sintering is traditionally used for manufacturing ceramic objects, and has also found uses in such fields as powder metallurgy.

A number of low-temperature sintering techniques, enabled by a nanoscale silver paste, have been developed for attaching large-area (>100 mm²) semiconductor chips. These developments address the need of power device or module manufacturers who face the challenge of replacing lead-based or lead-free solders for high-temperature applications.

The solder-reflow technique for attaching large chips in power electronics poses serious concern on reliability at higher junction temperatures above 125°C. Unlike the soldering process that relies on melting and solidification of solder alloys, the typical low-temperature sintering technique forms the joints by solid-state atomic diffusion at processing temperatures below 275°C with the sintered joints having the melting temperature of silver at 961°C.

European electronic manufacturers, particularly those in power electronics, are aggressively implementing silver sintering technologies for interconnecting semiconductor chips. It has been shown that power modules with sintered chip-attachment have 3x better performance, 5x better reliability, and higher chip junction temperature up to 175°C. However, because of the use of commercial thick-film silver pastes in the process, a serious drawback of the sintering technology is the need of a high quasistatic pressure (~ 40 MPa) to lower the sintering temperature to about 250°C. Using the large pressure complicates the manufacturing process and places critical demands on substrate flatness and chip thickness.

Heraeus has developed a novel concept for silver sinter pastes. The new concept uses micro scale silver particles combined with sinter additives. The novel pastes have high sinter activity and can be used in pressure free or less pressure bonding processes. The physical properties like shear strength at temperature above 200°C, electrical and thermal conductivity are outstanding compared to solder or silver adhesives. The new paste concept can reduce the pressure for the “Low Temperature Joining Technology” and is an alternative to nano-scaled silver pastes and can be potential lead free solutions for die attach applications.

d) Transient Liquid Phase (TLP)

For the assembling and mounting of temperature sensitive micro-components, a low temperature joining process, like the Transient Liquid Phase (TLP) bonding, is needed. The TLP-Bonding process combines the characteristics of liquid-phase joining (soldering and brazing) with diffusion bonding.

Diffusion Bonding- • Background

Diffusion bonding is a solid to liquid interdiffusion bonding process, that is now a highly accepted Pb-free technology based on isothermal solidification. It involves use of a low melting metal sandwiched between high melting metal layers. When heated under a small amount of applied pressure Intermetallic compounds (IMC) are formed. The IMCs show a drastic changes in thermal, electrical and mechanical behaviour.

TLP Bonding is a process of diffusion Bonding without the application of pressure. It is a low temperature joining process for materials like ceramics, synthetic materials or metals, particularly for the assembling and mounting of temperature sensitive micro-components. The TLP system is a binary multilayer system of thin films. One film possesses a high (e.g. Cu, Au) and the other a low (e.g. Sn, In) melting point. During heating, the low melting component diffuses into the high melting component and forms an intermetallic phase, raising the remelting temperature of the system.

The multilayer system can be deposited by a PVD process.

Some TLP with Cu-Sn and Cu-In show high potential for joining operations in microsystems. The benefit of these systems is the combination of the low melting elements to the eutectic alloy Sn-In.

Typical Liquid Phase Joining process:

Fusible metal alloy >450°C.

Application of heat to reflow braze alloy.

Braze metals with/without metallisation.

Ceramics, usually metallised (e.g. Mo/Mn, Sputter coating, thick film).

Ceramics can be brazed directly using active braze materials (e.g. Ti additive).

Requires flux or a protective atmosphere.

Application of heat and pressure in an oxygen rich environment.

Copper oxidises and forms eutectic liquid (Cu₂O) at 1070°C.

Reference:

“LT-TLPS Die Attach for High Temperature Electronic Packaging”

by Hannes Greve and Patrick McCluskey,

CALCE/Department of Mechanical Engineering

Clark School of Engineering, University of Maryland

at HiTEN 2013 - July 8-10, 2013.

Low Temperature Transient Liquid Phase Sintering (LT-TLPS) is also referred to as Solid-Liquid Interdiffusion Bonding (SLID).

System of constituent A with a low melting temperature T_1 and constituent B with a high melting temperature T_2 The paste is processed at $T_1 < T_p < T_2$ where A melts and wets B. Intermetallic compounds are formed with a melting temperature above T_1 .

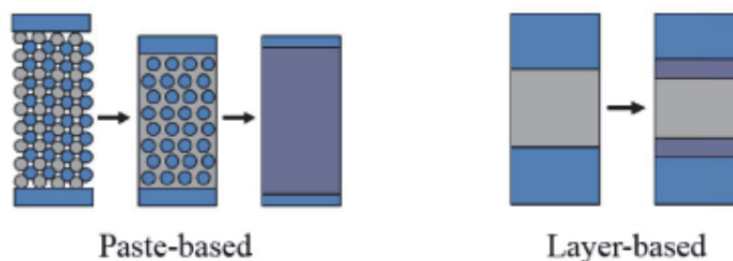
The chart below shows an example of typical solder and intermetallic values.

Die Attach Material	SAC305	High-T Solder	Cu ₆ Sn ₅	Cu ₃ Sn	Ag ₃ Sn
T _m	217°C	≈300°C	415°C	676°C	480°C
T _h at 125°C	0.81	0.69	0.58	0.42	0.53
T _h at 200°C	0.97	0.83	0.69	0.50	0.63
T _h at 250°C	1.07	0.91	0.76	0.55	0.69

T_m is the melt temperature of the solder. The homologous temperature T_h is an indicator for creep behaviour. Higher temperatures and therefore higher T_h reduce the fatigue life.

High-temperature solders (generally based on Pb- or Au-rich alloys) require processing at temperatures significantly above their melting temperatures. However, LT-TLPS joints can be formed at low process temperatures but enable high temperature application. Typical electronic system metallisations (NiPd, NiAu, NiCu, Cu, ENIG, ENEPIG, OS etc) can be joined where LT-TLPS joints can be formed pressure-less with a flux without vacuum and low cost material systems are available (Cu-Sn, Ni-Sn).

There are several layer-based TLPS systems available with Sn or In as the low-melting point constituent, these are (Ag, Au, Cu, Ni)-Sn, (Ag, Au)-In. One major disadvantage of the layer-based approach is the limited joint thickness due to the mechanics of the process, whereas controlling the formation of voids during sintering complicates the processing of LT-TLPS sinter pastes as shown in the diagrams below.



6) Bonding Process Issues

a) Die Attach Voids

Regardless of die attach process, the presence of voids in the die attach material affects the quality and reliability of the device itself. Large die attach voids result in low shear strength and low thermal/electrical conductivity, and produce large die stresses that may lead to die cracking. Small voids provide sufficient shear strength and electrical/thermal conductivity, while 'cushioning' large dice from stresses. Total absence of voids may mean high strength, but it may also induce large dice to crack.

The strength of die attachment is measured using the die shear test.

It is well known that the presence of voids will affect the mechanical properties of joints and deteriorate the strength, ductility, creep, and fatigue life. In addition, voids could also produce spot overheating, lessening the reliability of the joints.

Void vs. Die size has always been a historical issue in Module SMT. This could be because the flux does not have time to get out during the process flow and creates the void. The thicker the printed bondline, the less likely there is to be high level voiding. But if heated too long to get the flux boiling off then oxidation can occur which will also create voids. The application or process should quantify voiding criteria in terms of how large a void can be and how it impacts thermal performance.

This typically requires a DOE of type of flux, bondline thickness, length of dwelling in solder reflow profile, mesh of solder pellet...etc.

Good high heat dissipation is required throughout package life. To achieve this, the solder alloy needs to cover completely the surface between leadframe and die for good solder wetting on leadframe and die metallization, and low void rate on the die-attach layer. Typically, for power and high-power applications, maximum void rate allowed is 5%.

Note:

This voiding problem also appears on Surface Mount product like D2pak, Dpak, and QFN not just at die level. This issue will appear whenever soldering to a large surface area. Thermal pad voiding control at QFN assembly is a major challenge due to the large coverage area, large number of via, and low standoff.

Note; IPC – 7093 covers design & assy of bottom terminated components. It also lists test protocols.

Depending on die size a solution can be to use solder preforms in a pattern that will allow gases to escape while the solder flows and wets evenly. Another option is to dispense solder dots or squares to allow for enough coverage and solder volume to achieve good wetting and adequate solder fillet around the die; while volatile elements outgas.

Clean surfaces are extremely important.

As chip temperature climbs, shear stresses build up between all of the components both inside the package, and to the substrate. This is where adhesion makes a big difference. You need to ensure that the bond materials will wet and adhere well to all the internal metal and semiconductor surfaces, and of course that the package mount will wet the leads and, with a QFN, the centre pad, contact pads, and the substrate.

An atmospheric plasma surface preparation system (Ontos7) can be used to prepare the surfaces of your chip, leadframe, centre pad, contact pads, and substrate for ideal wetting of internal die attach, encapsulant, AND substrate mount. Shear tests of polymer adhesion show an increase in shear strength of 50% over vacuum plasma ashing and 100% over no surface prep at all.

Similar results can be achieved in soldering applications. The surface activation created with atmospheric plasma also helps greatly to eliminate voids in both adhesive and soldering applications.

b) CTE

Die attach can also provide a level of CTE matching between die and substrate providing a resistance against thermal fatigue.

During package life, the joint is subjected to cyclic heating and cooling. The mismatch in coefficient of thermal expansion (CTE) between the die and the leadframe induces shear stress, which leads to so-called thermal fatigue in the joint. The die-attach layer needs to withstand thermal fatigue to ensure joint reliability.

Low-power devices do not place as much CTE stress on the various components of the package. Power device operating temperatures do however. Table 2 indicates the variation in CTE of various power module substrates

**Table 2 - Summary of Key Properties for Typical Ceramic Substrates
(Courtesy Kyocera) "Power Electronic"**

Material		Thermal properties		Mechanical properties		Conductor material	Plating options	Sheet resistivity	Printed resistor
		CTE	Conductivity	Strength	Youngs Modulus			Ω/sq	
		ppm/ $^{\circ}\text{C}$	W/mK	Mpa	Gpa				
Alumina	A440	6.9	18	400	270	W, Mo	NiAu	8-13m Ω/sq Plated 4m Ω/sq	Yes
	A473	7.1	14	400	310	W, Mo	NiAu NiPdAu	8-13m Ω/sq Plated 4m Ω/sq	Yes
	AO630	7	16	460	275	CuW, Mo	NiAu NiPdAu	Fine - 5m Ω/sq Standard - 3m Ω/sq Power - 1.5m Ω/sq	Yes
AlN	AN242	4.7	150	400	320	W	NiAu	8-13m Ω/sq Plated 4m Ω/sq	Yes
LTCC	Du Pont 951	5.8	3.3	320	120	Au, Ag	-	5-10m Ω/sq (Au) 2m Ω/sq (Ag)	Yes
Si ₃ N ₄	SN460	2.7	58	850	300	Cu	Ni, NiAu NiPdAu, NiPdAg	-	No

High-lead alloys withstand thermal fatigue stress because they are soft, have a wide elastic deformation range, and can survive plastic deformation. This allows them to compensate the shear stress induced in the die-attach layer. Additionally, the finer the alloy micro-structure directly after reflow and during the package lifetime, the slower fatigue crack propagation, and the more reliable the die-attach joint. Unfortunately, alloys with the finest micro-structures are more prone to oxidation, and therefore more difficult to handle and process to achieve good wetting and low void rate. Thus, the best solder alloy for a given application is always the best compromise between reliability requirements and processing requirements.

A suitable substitute for high-lead solder alloys requires: material processing at temperatures below 400 $^{\circ}\text{C}$; no re-melt until a temperature of at least 260 $^{\circ}\text{C}$ is reached; good adhesion on conventional part surfaces; good resistance against thermal fatigue; and of course, no lead in the composition.

7) Replacements for "High-Lead" Solder Materials

A number of materials, covering the range of Eutectics TLP, Solders and Epoxies have been developed, claiming to be ideal "solutions" for high temperature lead free "solder". This section reviews the information of these and provides information about performance relating to the assembly of power devices into packages (and modules).

a) Ag-In materials:

Silver-Indium pastes are well known and have been used for a number of applications, giving an acceptable adhesion to both the die and substrate.

Refer to: Quintero, P., McCluskey, F.P., "Silver-Indium Transient Liquid Phase Sintering for High Temperature Die Attachment," J Microelectronics and Electronic Packaging, 6 (2009). pp.66-74.

Ag-In utilises process temperatures in the range 205°C to 300°C producing the phase required to form good intermetallics. The melt temperature T_m is $> 600^\circ\text{C}$, with a paste of approx. 32% by weight of Indium. This material is possibly the most expensive, but is the easiest processing and lowest temperature range.

b) Ag-Sn materials:

Generally, high-quality sintered silver joints must be processed with a combination of heating and the application of pressure. Sintering of non-noble metallization is complicated and produces joints with lower strength.

Ag-Sn and Cu-Sn Sinter Pastes are the current main types.

Ag as a noble metal does not easily form oxide, facilitating the sintering process. Ag-Sn pastes have a low process temperature as Sn melts at 232°C. The intermetallic compounds (IMCs) that are formed have good high melt temperatures (T_m). The chart shows the results using materials with Sn concentrations of 26.8% and 14.1% by weight.

IMC	ϵ (Ag_3Sn)	ξ (Ag_4Sn)
T_m	480°C	724°C
% Sn	26.8%	14.1%

c) Cu-Sn materials

The intermetallic compounds (IMCs) have a reasonably high T_m and are formed with materials having tin concentrations of 59% and 38% by weight, respectively. Higher concentrations of the tin-rich liquid phase facilitate process control, improve wetting, and reduce voiding. But a short, carefully controlled process duration is needed due to high diffusivity Cu being susceptible to oxidation.

IMC	η (Cu_6Sn_5)	ϵ (Cu_3Sn)
T_m	415°C	$>600^\circ\text{C}$
% Sn	59%	38%

The results from the work at Calce showed that paste based LT-TLPS process is viable using a range of sinter pastes based on the Ag-Sn and Cu-Sn. However for both types of pastes, there is a very long (relatively speaking) process time required of around 15 minutes, to enable the join to complete.

Ag20Sn joints show no reduction of shear strength up to 400°C. Yet their absolute joint strength is limited by the low content of liquid phases during processing.

Cu50Sn and Cu60Sn pastes showed high shear strength up to 400°C and 600 °C respectively. No critical drop of shear strength was found for the Cu-Sn pastes up to their respective application temperatures.(around 300°C) and so it was recommended that these materials can reliably be used for “attach” applications in high temperature electronic packages.

TLP Combination	Processing Temperature	Processing Time	Remelt Temperature
'Cu-Sn	280°C	4 min	>415°C
Sn-Ag	250°C	60 min	>600°C
'Sn-Ni	300°C	6 min	>400°C
Cu-In	180°C	4 min	>307°C
Ag-In	175°C	120 min	>880°C
Au-Sn	260°C	15 min	>278°C
Au-In	200°C	0.5 min	>495°C

NOTE:

The Process is not easy and if not carefully controlled, TLP Bonding can exhibit attachment inconsistency due to issues of:

- Processing time
- Temperature
- Surface cleanliness
- Surface roughness
- Curing profile
- Thermal stress developed

d) “Sintered Silver” epoxies

For use in Die attach processes, sintering of silver (Ag) particles comprises a silver powder applied between chip and substrate, which is pressed (> 40 MPa) under moderate temperature (> 250°C) to form a compact Ag joint. This low temperature joining technology (LTJT) provides high thermal and electrical conductivity as well as long lifetime of the modules at temperatures > 150°C.

However, in 2012 Heraeus noted that design and process constraints currently hamper the quick implementation in production lines, because special sintering presses are needed and the process is not compatible with pressure and temperature sensitive dies.

Since then new “pressure less” materials and new equipments have begun to come on stream (See Heraeus & Fico/Besi etc etc)

Sintered Ag die attach is of interest because:

- Processing temperature can be reduced to 300°C or less
- Applied pressure not needed during sintering (depending upon materials !)

i) Material 1 - NBEtech – NanoTach

NanoTach® is a thick paste of nano-sized silver powder in an organic binder that can be used as an alternative to solder or epoxy in semiconductor devices in the state-of-the-art individual packages or multi-chip power modules. NBE's lead-free nanomaterial attachment possesses better thermal, mechanical and electrical properties than soldered or epoxied alternatives. The attachment process is completely compatible with existing equipment and facilities that use solders or epoxies. Using NBE's material and process, high power-density semiconductor electronic or optoelectronic devices can be operated at high temperatures in excess of 250° C, not attainable with any existing solder-based or epoxy-based materials. Specific applications can include bonding to large chips for power devices/modules, high-power and high-brightness LED lamps, power diode lasers, and RF power devices.

Compared to the current die-attach materials, nanoTach® offers:

- 5x higher thermal and electrical properties
- > 250° C capability
- < 275° C ambient or low pressure (5 MPa) processing
- Improved reliability from low elastic modulus
- One-to-one RoHS compliant replacements.

The NanoTach N nano particle silver paste.

Process: Manual paste dispense, Die placement with orbital scrub to 40-50 um wet

Bondline. 20 h room temp air dry. Use of manufacturers recommended dry & sinter profile to 300C peak. – a 2.5hr process time.

(No pressure required up to 3mm sq surface area)

Summary of tests carried out by ELTEK (from report at HiTen 2013).

1. Au substrate provides good initial contact to sintered Ag but over time Au diffusion into the Ag leads to a layer of voids which weakens the joint.
2. Fast Au diffusion related to the high density of grain boundaries in the sintered material.
3. Ag substrate shear strength increases with ageing due to higher interfacial contact area and disappearance of the small voids with time.
4. High porosity region at edge of die extends ~ 100 um.
5. Possible issue with Ni/Ag plating is used on die

NanoTach® (nanosilver paste): X Series “Silver Sintering Die-attach at Zero Pressure”

Product Description

Thick paste of nano-sized silver powder in an organic binder formulation.

Key Features

- Uniform dispersion for screen/stencil printing or dispensing
- Low sintering temperature (<260oC)
- Excellent sintered properties
- RoHS compliant

Applications

Bonding small to large chips (over 10mm x 10mm) for power devices/modules, high-power and high-brightness LED lamps, power diode lasers, RF power devices.

Typical Properties

Physical Data Before Sintering:		Physical Data After Sintering	
Color:	dark gray	Porosity:	< 30%
Solid loading:	71 - 91%	Density:	> 7.9 g/cm ³
Density:	> 3.0 g/cm ³	CTE (coefficient of thermal expansion):	19.6 x10 ⁻⁶ /°C
Viscosity:	150,000 to 600,000 cps	Melting temperature:	961°C
Sintering temperature:	< 260°C	Elastic modulus:	~ 10 to 30 GPa
Shelf life ¹ :	~ 12 mo.	Electrical resistivity:	< 2.6x10 ⁻⁶ Ω•cm
		Thermal conductivity ² :	> 2.0 watt/cm•°C
		Chip bonding strength:	> 25 MPa
¹ If stored in sealed containers at room temperature		² Calculated from electrical measurement	

Properties of NBE's nanoTach® Material				
	NBE's nanoTach®	High-lead solder (95Pb-5Sn)	Eutectic Gold-tin solder	Hysol® QMI 3555R
Processing temperature	< 280°C	340°C	320 – 340°C	300 – 450°C
Maximum use temperature	<961°C (mp of Ag)	<280°C	< 280°C	< 250°C
Bonding shear (MPa)	20 – 40	15	> 100	20
Elastic modulus (GPa)	9	19	80	11.5
Electrical conductivity, 10⁵ (Ω•cm)⁻¹	3.8	0.45	0.625	6.7x10 ⁻⁷
Thermal conductivity (W/K•m)	240*	23	58	80
RoHS Compliance Status	Compliant	Not Compliant	Compliant	Compliant

*Estimated based on electrical resistivity measurement.

Note:

Henkel brand Hysol QMI 3555R is a no-dry Ag/glass die attach for glass, solder and sealed packages.

ii) Material 2 – Henkel

Henkel's LOCTITE ABLESTIK SSP-2000 is a printable low temperature silver sintering paste die attach adhesive designed for devices requiring high thermal and electrical conductivity. It is formulated to provide high heat transfer generated from power devices. It maintains high adhesion at operating temperatures as high as $\geq 260^{\circ}\text{C}$.

From the data sheet, the following should be noted:

Recommended Sintering Profile

30 minute ramp from 25°C to 250°C + 60 minutes @ 200°C

Alternative Sintering Profile

30 minute ramp from 25°C to 220°C + 60 minutes @ 220°C

Recommended Sintering Profile for Different Die Sizes

$\leq 5 \times 5$ mm die on PPF or Ag LF:

Sinter in air 30 min ramp to 250°C + 1 hour @ 250°C

Sinter in air 30 min ramp to 200°C + 1 hour @ 200°C

Sinter in nitrogen 30 minute ramp to 250°C + 1 hour @ 250°C

6×6 mm die on DBC substrate:

Sinter in air 30 minute ramp to 200°C + 1 hour @ 200°C

LOCTITE ABLESTIK SSP 2020 is a sintering silver paste die attach adhesive designed for devices requiring high thermal and electrical conductivity. It is formulated to provide high heat transfer generated from power devices. It maintains high adhesion at operating temperatures as high as 260°C . It is stencil printable and syringe dispensable. It has a Thermal Conductivity $>100 \text{ W}/(\text{m-K})$.

From the data sheet, the following should be noted:

“Pressureless” Sintering Process:

A) Ag or Au Leadframe - sintered in:

Conventional Air Circulated Oven

10 minute ramp to 250°C

+ 60 minutes @ 250°C

N2 Oven

10 minute ramp to 250°C

+ 60 minutes @ 250°C

B) Direct Bonded Copper (DBC)

on Au:

10 minute ramp to 200°C

+ 60 minutes @ 200°C

on Ag:

10 minute ramp to 250°C

+ 60 minutes @ 250°C

Pressure Sintering Process

Air dry 40 minutes @ 120°C then sinter 2 minutes @ $\geq 250^{\circ}\text{C}$ at $>10 \text{ MPa}$ pressure

The above sintering profiles are guideline recommendations. Sintering conditions (time and temperature) may vary based on customers' experience and their application requirements, as well as customer sintering equipment, oven loading and actual oven temperatures.

iii) Material 3 – Heraeus Materials - “MAGIC” microbond

Heraeus have been developing a range of Low temperature Sinter(LTS) paste materials based upon the silver sintering process to suit specific market needs:

- C 1075 S – Early product
- LTS 016 – pressure sinter material
- LTS 043 - a pressure sinter
- LTS 116 - a Low pressure sinter
- LTS 174 – a Low pressure sinter
- LTS 295 – a Low pressure sinter

Silver Paste	Sintering Conditions	Produced Apparent Bulk Density (g/cm ³)	Produced % of Full Density [†]
	T = sintering temperature S = uniaxial compressive stress t = time under stress		
C 1075 S	T = 250°C, S = 50 MPa, t = 10 min	6.46	62.1
LF131	T = 350°C, S = 50 MPa, t = 10 min	8.41	80.9
	T = 350°C, S = 50 MPa, t = 10 min	8.42	81.0
LTS 016	T = 350°C, S = 50 MPa, t = 25 min	10.07	96.8
LTS 043	T = 350°C, S = 50 MPa, t = 25 min	9.66	92.9
	T = 350°C, S = 50 MPa, t = 25 min	10.03	96.4

[†] Theoretical density of silver = 10.4 g/cm³.

Processing conditions of the materials – Courtesy Oak Ridge National Laboratory/OSTI
An example comparison of LTS material performance, from CPES

Property		UNIT	High Lead Solder	Heraus Silver Paste (LTS116)	Ni-Sn Metal Alloy
Coefficient of Thermal Expansion (CTE)		ppm/°C	29	19	8.65
Thermal Conductivity	at 25 °C	W/m-°C	26	240	19.6
Maximum Service (Reflow) Temperature		°C	300	961	400
Electrical Resistivity	at 25 °C	Ω-cm	2.01E-07	6.67E-08	2.85E-07
Electrical Conductivity		S/m	4.98E+06	1.50E+07	3.51E+06
Tensile Strength		MPa	29	55	
Shear Strength		MPa	15.4	10-20	
Solid Content		%		89	
Viscosity		cPs		35000-50000	
Processing Temperature (lowest)		°C	300	220	250
Processing Time (correspond to Processing Temp)		min		50	
Print Thickness		µm		40-150	
Shelf Life (at 4°C)		Month		6	

NOTE:

These materials listed above were being “developed” in special projects, and were not readily available to the market without special conditions being applied to the work undertaken. The materials have been used in test programmes and research projects. Therefore only a very limited amount of product data is available.

Heraeus have replaced/upgraded the above Silver Sinter materials in the new range of “mAgic” microbond silver interconnect pastes.

This Microbond Ag Interconnect mAgic product family utilizes the “sintering technology”. They are now promoted to support power electronics as the key requirements for the interconnects on DCB substrates are increased lifetime, low thermal resistance and elevated operation temperature.

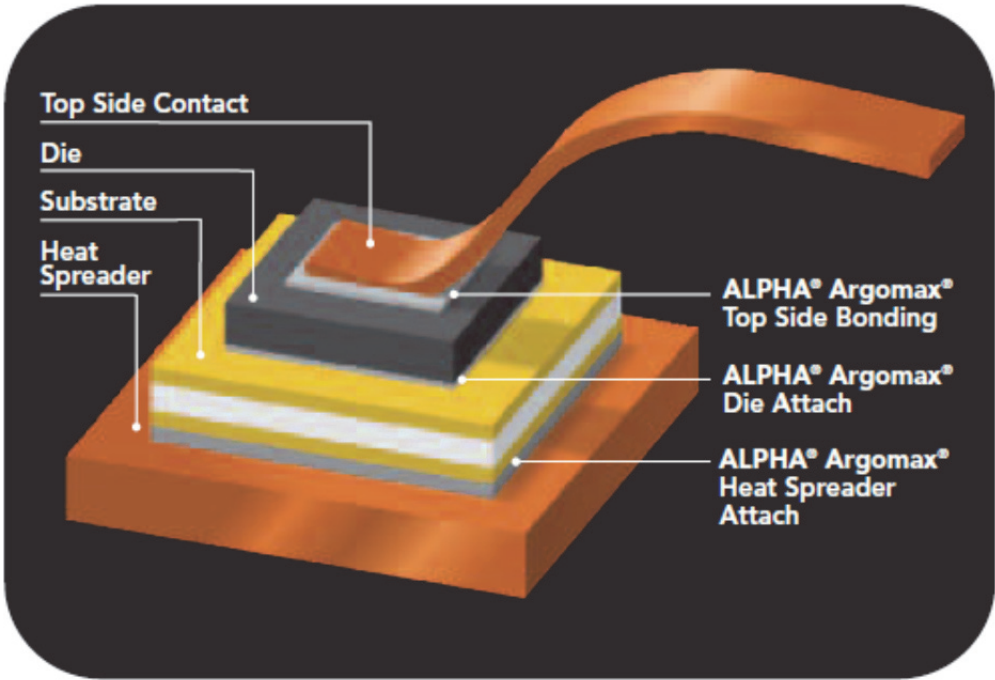
Series	Conventional Conductive Adhesive	mAgic Adhesive	mAgic Paste	Solder
Process Temperature	120 – 175 °C	180 – 200 °C	200 – 280°C	200 – 350 °C
Max. Operation Temperature	150	200	> 250	150
Electrical Resistivity (mΩ-cm)	≤ 0.1	≤ 0.05	≤ 0.008	0.01 – 0.03
Thermal Conductivity (W/mK)	2 – 7	> 30	> 100	20 – 50
CTE (ppm/K)	40/100	50/110	≤ 23	25 – 30
E-Modulus @ 25 °C (GPa)	1 – 4	4	> 35	~ 30

	mAgic Adhesive	mAgic Paste		
	No Pressure ASA	Pressure Assisted ASP043	Pressure Assisted ASP131	No Pressure ASP295
Application				
Die Attach	+	+	+	+
Component Attach	+	n/a	n/a	+
Process				
Dispensing	+	n/a	n/a	+
Printing	+	+	+	+
Properties				
Halogen Free	+	+	+	+
Lead Free	+	+	+	+
Recom. Sinter Pressure	0 MPa	20 MPa	10 MPa	0 MPa
Sintering in Air	+	+	+	+
Sintering in N ₂	+	n/a	n/a	+
Cleaning	not needed	not needed	not needed	not needed
Metal Content after Processing (by weight)	89%	100%	100%	100%
Compat. Surface Finishes				
Ag	+	+	+	+
Au	+	+	+	+
Pd	+	+	+	+

Full application information for these products is now being made available by Heraeus.

iv) Material 4 – Cookson “Argomax”

Power modules made with Argomax® Sinter Technology meet the increasingly challenging requirements of today’s and tomorrow’s power generation and consumption applications.



ARGOMAX® sinter technology from Alpha® was specifically developed for low pressure, high speed sintering enabling cost effective die attach. It is formulated using highly engineered particles, manufactured by Alpha®.

ARGOMAX® provides high thermal and electrical conductivity silver bonds between die and substrate, good adhesion and flexible bond line thickness. It has consistent performance and excellent shelf life.

Argomax® Sinter technology overcomes the challenges of thermal management and electrical performance under the harsh conditions that power electronics faces. It is sintered at low temperatures with short processing times which makes it economically viable for high volume manufacturing environments. The enhanced structure of Argomax® improves mechanical properties and thermal fatigue resistance.

Argomax® sinter paste or film quickly converts to bulk silver through the sintering process. The onset of this process is 150°C and takes very little time to convert to micron particles. They then convert to bulk Ag through grain growth and densification, as temperature and time increases. This occurs even without applied pressure. When you perform sintering under recommended conditions, a dense metal film is formed, with strength comparable to bulk silver.

Comparison of ALPHA® Argomax® to key alloys on the market:

		92.5Pb/2.5Ag/5.0Sn	SAC 305	Argomax®
Thermal Conductivity	W/(K•m).	25 – 27	59	200-300
Electrical Resistivity	μohm/cm	14 -17	10	2.5-3.5
CTE	ppm/°C	29	7	18

For Si/SiC/GaN die attach processes Argomax® offers:

- Low process temperatures from 190°C to 300°C
- Recommended sintering pressure 5-10 MPa or higher
- High thermal conductivity silver bond line from 200-300 W/m²K
- Dies from <1mm² to wafers >70,000mm²
- Bondline from 5 um to 100 um
- Lead free
- Zero voiding
- Long shelf life at room temperature

Argomax® Sinter Technology

TECHNICAL PROPERTIES

Granulometry 20nm

Rec. Processing Temp. 190-300°C

Thermal Conductivity 200-300W/mK

Electrical Resistivity 2.5-3.5 µhm/cm

CTE 18 PPM/°C

Report back of work with Argomax by user “X”: (Withheld name due to NDAs)

Cookson supplied “X” with two of their Argomax products. One was a silver nano paste suitable for bonding to silver (known as 2020), the other a silver nano paste suitable for bonding to copper (known as 5020). Both these products have a particle size of approximately 20 nm.

The onset temperature for sintering these pastes is 150°C, but a high pressure is necessary at these temperatures. To reduce the pressure requirement a higher temperature is needed to obtain a good sintered bond. For both materials the recommended processing schedule was:

- i) print the paste onto the substrate,
- ii) dry the paste at 130°C for 30 minutes to lose volatiles
- iii) add “tophat”
- iv) apply pressure
- v) sinter at 250°C for 3-5 minutes
- vi) post cure at 250°C without pressure for 30 minutes to improve thermal and electrical conductivity

The result was acceptable.

Following trials and process reviews, a pressureless approach with Heraeus silver paste LTS 295-26P2 was adopted

v) Material 5 - DuPont

Dupont materials are involved paste products for Thin and Thick film hybrids and LTCC products which use silver pastes and a “patented” sintering process.

LF131 (see note in early Heraeus section)

DuPont LF131 silver conductor composition is intended to be applied to ceramic substrates by screen printing and firing in a conveyor furnace in an air (oxidizing) atmosphere. It has been developed to form interconnection tracks and pads for component and lead attachment, in hybrid microcircuits and networks.

It is not a viable product for use in a sintered silver die attach process

vi) Material 6 – GEM UK

Gwent Electronic Materials (“GEM”), it has developed a new range of more conductive Silver/Silver Chloride Pastes, in a different ratios with the same Silver content.

They are suppliers of nanoparticle silver powders and pastes. They are working with Microsemi, and NPL UK in a UK TSB funded project “ ELCOSINT”. This project is based upon silver sintering pastes for pressure less die attach processes.

They have not yet released any details of this work

e) Bismuth/Silver

Bismuth (Bi) is being used more and more as a replacement for lead in solder alloys because it is non-toxic. Although the melting temperature of pure bismuth is 271°C, the addition of bismuth will lower the melting temperature of most metals it is alloyed with.

Bismuth/silver (BiAg) alloys are claimed to be a drop-in solution for replacement of high-lead solders. Alloys containing between 2 and 12% silver (Ag) satisfy the requirements of melting temperature.

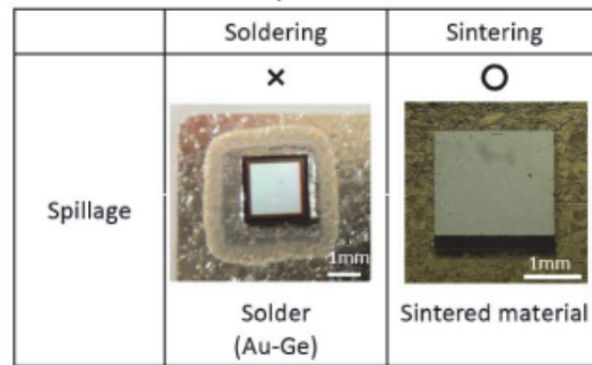
Indium Corp., offer a range of solders. Indalloy® 261, Indalloy 281 and 282. They have joint properties similar to those of tin-lead solders, with superior fatigue and copper dissolution characteristics. However Bismuth is the most diamagnetic and the least thermally conductive of all metals and in addition to being non-toxic it does not oxidize as readily as lead does.

Unfortunately, from a number of references, it seems that the wetting on copper (Cu), which is a popular metallization type, is very limited. Also, the low thermal conductivity of the alloy may lead to die overheating and damage. The manufacturing conditions of the alloy are problematic, because a high deformation speed leads to a brittle response.

For these reasons, BiAg alloys do not fully match the requirements for substituting high-lead-containing solders.

f) Gold sinter paste

Use of Sintered materials gives a far better performance in terms of die attach “spillage” or edge spread.



Joint material without short circuit
→ Sintered material

Reference: *National Institute of Advanced Industrial Science and Technology (AIST)* –

Submicron Au paste - see <http://pro.tanaka.co.jp/topics/fileout.html?f=83>

Type: - AuRoFUSE™ TR-191R from Tanaka

Material format:

- : 0.1 ~ 0.5 μm Au Particle
- Au content: 95wt%
- Viscosity: 886Pa's
- NO binder resin

Characteristics

- Sintering joint temperature ~ 200°C
- Available for chip by chip joint process without any re-melt phenomena (Melting point T_m after sintering: 1064°C)
- Anti-oxidation stability in air environment

Note: Problem of the Ni-Oxide layer on the substrate (Chip) electrode, as this can block the Au-Au bonding between electrodes and Au particles In order to avoid this problem, pre-sintered Au paste has to be applied to both surfaces before attach process. (costly process)

8) Measurement Requirements

Inevitably a number of parameters concerning the characteristics of a device/package/board assembly need to be ascertained in order to provide the necessary data to validate and match specific application needs.

As device/package /board modelling is now a key feature of new electronic system design the whole aspect of device parameter measurement is of fundamental importance. Accurately measured parameter references are used to ensure optimum performance, reliability and lifetime of the overall system.

For an example of basic measurement aspects, refer to :

Texas Instruments Application report of 2004 : AN-1205 Electrical Performance of Packages

<http://www.ti.com/lit/an/snoa405a/snoa405a.pdf>

This document gives examples of how different package types R-L-C values vary.

The introduction of new solder materials will mean development of test methods and measurements in order to provide complete “component” data for modelling.

The key parameters and their measurement method are as follows:

a) Resistance

Resistance is the cause of IR drops in the package. DC resistance is the resistance of a conductor when the entire cross section of the conductor is carrying current. At higher frequencies, the current is concentrated along the surface of the conductor, due to skin effect. AC resistance increases with frequency, because as the frequency increases, skin depth decreases, and the available cross section for the current flow decreases. AC resistance varies linearly with length of the conductor, but not with respect to cross sectional area.

Basic physical methods of measurement can be used.

The EIA/Jedec standard JEP126 can be applied but defines values by computational analysis.

b) Inductance

Inductance (L) is defined as the relationship between the following for a closed current path:

- flux linkage (λ) and current flow (i): $\lambda = L \times i$ or
- time varying voltage (v) and current (i): $v = L \times di/dt$

Measurements are defined in Jedec JEP123 – Guideline for Measurement of Electronic Package Inductance and Capacitance Model Parameters:

c) Capacitance

Self capacitance is the capacitance of any element to "ground". In package electrical models, the plane on the PC board is assumed to be an ideal ground. Thus, self capacitance of any package element is the capacitance of that element to the board plane. Mutual capacitance is the capacitance between any two elements. For example, in a lumped model of ball grid array package, capacitance from a package trace to the package VSS plane is mutual capacitance.

Apply Jedec JEP123 – Guideline for Measurement of Electronic Package Inductance and Capacitance Model Parameters:

d) Thermal Cycling

Apply JC-15 standards for Temperature Cycling (JEDEC Standard No. 22-A104D)

And review:

Methodology For The Thermal Measurement Of Component Packages (Single Semiconductor Device) JESD51 (Dec 1995)

This standard and its subsequent addendum's, provides a standard for thermal measurement that, if followed fully, will provide correct and meaningful data that will allow for determination of junction temperature for specific conditions. The data can be used for package design evaluation, device characterization and reliability predictions.

e) Shear test

Shear Testing is the process of determining the strength of adhesion of a semiconductor die to the package's die attach substrate (such as the die pad of a lead frame or the cavity of a hermetic package), by subjecting the die to a stress that's parallel to the plane of die attach substrate, resulting in a shearing stress between: 1) the die-die attach material interface; and 2) the die attach material-substrate interface.

Apply: Die Shear Testing - Mil-Std-883 Method 2019

Package to board shear test is now becoming a similar process due to small package sizes. Test process above is applicable for ECP and PQFN packages.

However this tends to be a solder joint test, not a packaging strength test.

Note:

For wire bonds and particularly wafer “bumps” Cavity Shear testing has recently been introduced. The method was developed to improve the quality of data obtained during gold ball bond shear testing, and it is useful to compare existing chisel-based shear test methods to the new cavity shear approach. The “chisel” tool is replaced by a “cavity” tool in the test equipment.

Bond strength per unit area will only continue to increase as bumps on wafers and chip scale packages continue to decrease in size. Therefore, the cavity shear test could quickly supersede existing shear test techniques as they increasingly fail to deliver an acceptable level of test accuracy and reliability in gold ball bond testing.

f) Current Densities

Current density is the electric current per unit area of cross section. It is defined as a vector whose magnitude is the electric current per cross-sectional area at a given point in space (i.e. it's a vector field). In SI units, the electric current density is measured in amperes per square metre.

A device maximum current density is normally provided by the manufacturer and depends upon chip geometries etc. A common average for 180 nm technology is $1\text{mA}/\mu\text{m}^2$ at 25°C . Above a maximum current density, apart from the joule effect, some other effects like electromigration appear in the micrometer scale.

g) Thermal Resistance

Thermal resistance is a heat property and a measurement of a temperature difference by which an object or material resists a heat flow (heat per time unit or thermal resistance). Thermal resistance is the reciprocal of thermal conductance.

- Thermal resistance R has the units $(\text{m}^2\text{K})/\text{W}$.
- Specific thermal resistance or specific thermal resistivity $R\lambda$ in $(\text{K}\cdot\text{m})/\text{W}$ is a material constant.
- Absolute thermal resistance R_{th} in K/W is a specific property of a component. For example, R_{th} is a characteristic of a heat sink.

Apply:

1. MIL-STD-883E-1012.1, Test Method Standard, Microcircuits, Thermal Characteristics.
2. EIA/JEDEC, JESD24-3, 24-4, 51, 51-1 through 51-8.

h) Thermal management – performance measurement

Jedec JC-15 has created several new thermal metrics. The first, the junction-to-board thermal resistance (Q_{JB}) is useful in estimating the temperature difference between the junction temperature of an IC and that of the PCB at the center lead location of the package. As such, unlike Q_{JA} , it actually has some utility in estimating the junction temperature in an actual application when the board temperature is known and most of the heat dissipated in the package flows to the ambient air by way of the board. In the situation in which a fraction of the dissipated heat flows to the board, then the use of Q_{JB} provides a conservative estimate of the junction temperature.

The various “Theta” values are supplemented by “Psi” values, such as Y_{JB} and Y_{JT} . Unlike “Theta” values, that are measured in environments in which nearly 100% of the dissipated power flows from the junction to the indicated reference temperature location, the “Psi” values are measured in environments in which only a portion of the dissipated power flows to the indicated reference temperature location. The “Psi” values are not true thermal resistances and are referred to as Thermal Characterization Parameters. The “Psi” values can be of value in estimating the junction temperature in convection cooling environments in which there is no heat sink attached to the top of the package.

See Jedec JESD51-12 — Guidelines for Reporting and Using Electronic Package Thermal Information. This is the basis for measurement as it includes:

- Thermal measurement method
 - Electrical test method
- Thermal environment
 - Natural convection chamber
 - Forced air (i.e.: wind tunnel)
 - Junction-to-board thermal resistance cold plate
- Component mounting (i.e.: test board)
 - Test board design extension to accommodate an exposed pad direct attach mechanism

The key relevant documents are

- JESD15: Thermal Modeling Overview
- JESD15-1: Compact Thermal Model Overview
- JESD15-3: Two-Resistor Compact Thermal Model Guideline
- JESD15-4: DELPHI Compact Thermal Model Guideline
- JESD15-5: CTM Package Thermal Data (PTD) Interchange File Format (IFF). (This is intended to enable the efficient transmission of CTM parameters from machine to machine.).

i) Intermetallic processes

There is no process currently “standardised” to measure this parameter.

j) Surface Finishes

It is known that various substrate finishes affect performance of many of the package aspects, however there is no work currently underway to define the effects and understand what “measurable” parameters are needed.

9) High temperature Solder projects in Consideration:

CONNECT –On line list a number of project proposals for consideration in H2020:

a) robust damage models for the newer high temperature Pb-free solders (HiRel, Innolot, Nanosilver).
..... **DfR Solutions (USA)**

b) reliability of new soldering material (alloys or adhesives).?
..... **Politecnico di Bari.(Italy)**

c) -High temperature solder alloys (no pb or au)

d) -silver sintering with die-placement equipment (pressure assisted or pressure less)

e) -Temperature dependent Material characterization (nanoindentation, tensile tests, etc. up to 300°C)

f) - reliability tests (power cycling, passive temperature cycling, humidity, vibration) with lifetime modeling (FEM)

g) -power electronics on pcb boards (reliability and lifetime tests)

h) -new wire bonding materials (copper heavy wire, al-cu, silver ribbons)

..... **Fraunhofer IISB (Germany)**

j) High temperature solders reliability

k) Damage evolution models for lead free solder(thermal and isothermal).

..... **Tennessee Technological University (USA)**

l) - High temperature solder joints

m) - Void-free Large area die-attach solder connections

n) - Diffusion soldering

o) - Solder process optimization and advanced soldering mechanisms

p) - Sintering process (all variants)

q) - Heavy thick wire bonding (up to 500um) (copper, copper-clad and ribbon)

r) - Module constructions and practical implementation for drive and lighting applications

s) - Reliability assessments

t) - Simulation models for lifetime assessment and failure criteria

u) - Benchmarking and comparison with other power electronics packaging technologies

..... **University of Erlangen-Nuremberg (Germany)**

v) - solder materials rheology study, e.g. solder paste rheology, which impacts on the printing greatly and then impact on reflow, post-reflow accordingly.

..... **Kester components Pte Ltd (S'pore)**

w) - high temp soldering

x) - effective consumption of raw materials - substitution of In, Ag, Au in Pb-free soldering

y) - soldering from macro- to micro- and nano scale

z) - the development of devices and testing procedures for characterization of solder joint reliability.

.....**Centre for High Temperature Studies at Foundry Research Institute (Poland)**

Sub-Appendices

Appendix 1: RoHS exemptions

RoHS 2 – Exemption list (from RSL technical consulting):

See: <http://www.rsjtechnical.com/WhatareRoHSexemptions.htm>

1	MERCURY in single capped (compact) fluorescent lamps not exceeding:
1a	For general lighting purposes < 30 W: 5 mg per burner. <i>Expired December 31, 2011</i> After December 31, 2011: 3.5 mg per burner After December 31, 2012: 2.5 mg per burner
1b	For general lighting purposes ≥ 30 W and < 50 W: 5 mg per burner <i>Expired December 31, 2011</i> After December 31, 2011: 3.5 mg per burner
1c	For general lighting purposes ≥ 50 W and < 150 W: 5 mg per burner
1d	For general lighting purposes ≥ 150 W: 15 mg per burner
1e	For general lighting purposes with circular or square structural shape and tube diameter ≤ 17 mm. <i>No limit until 2012</i> After December 31, 2011: 7 mg per burner
1f	For special purposes: 5 mg per burner
2a	MERCURY in double-capped linear fluorescent lamps for general lighting purposes not exceeding:
2a1	Tri-band phosphor with normal lifetime and a tube diameter < 9 mm (T2): 5 mg per lamp. <i>Expired December 31, 2011</i> After December 31, 2011: 4 mg per lamp
2a2	Tri-band phosphor with normal lifetime and a tube diameter ≥ 9 mm and ≤ 17 mm (T5): 5 mg per lamp. <i>Expired December 31, 2011</i> After December 31, 2011: 3 mg per lamp
2a3	Tri-band phosphor with normal lifetime and a tube diameter > 17 mm and ≤ 28 mm (T8): 5 mg per lamp. <i>Expired December 31, 2011</i> After December 31, 2011: 3.5 mg per lamp
2a4	Tri-band phosphor with normal lifetime and a tube diameter > 28 mm (T12): 5 mg per lamp. <i>Expires on December 31, 2012</i> After December 31, 2012: 3.5 mg per lamp
2a5	Tri-band phosphor with long lifetime ($\geq 25\,000$ h): 8 mg per lamp <i>Expired December 31, 2011</i> . After December 31, 2011: 5 mg per lamp

2b MERCURY in other fluorescent lamps not exceeding:

2b1 Linear halophosphate lamps with tube > 28 mm (T10 and T12):
10 mg per lamp *Expires on April 13, 2012*

2b2 Non-linear halophosphate lamps (all diameters): 15 mg per lamp
Expires on April 13, 2016

2b3 Non-linear tri-band phosphor lamps with tube diameter > 17 mm (T9)
No limit until 2012. After December 31, 2011: 15 mg per lamp

2b4 Lamps for other general lighting and special purposes (induction lamps)
No limit until 2012. After December 31, 2011: 15 mg per lamp

3 MERCURY in cold cathode fluorescent lamps and external electrode fluorescent lamps (CCFL and EEFL) for special purposes not exceeding:

3a Short length (≤ 500 mm). *No limit until 2012*
After December 31, 2011: 3.5 mg per lamp

3b Medium length (> 500 mm and $\leq 1,500$ mm). *No limit until 2012*
After December 31, 2011: 5 mg per lamp

3c Long length (> 1 500 mm). *No limit until 2012*
After December 31, 2011: 13 mg per lamp

4a MERCURY in other low pressure discharge lamps. *No limit until 2012.*
After December 31, 2011: 15 mg per lamp

4b MERCURY in high pressure sodium (vapor) lamps for general lighting purposes in lamps with improved color rendering index $R_a > 60$ not exceeding:

4b-I $P \leq 155$ W. *No limit until 2012.* After December 31, 2011: 30 mg per burner

4b-II $155 \text{ W} < P \leq 405 \text{ W}$. *No limit until 2012*
After December 31, 2011: 40 mg per burner

4b-III $P > 405 \text{ W}$. *No limit until 2012.* After December 31, 2011: 40 mg per burner

4c MERCURY in other high pressure sodium (vapor) lamps for general lighting purposes not exceeding:

4c-I $P \leq 155 \text{ W}$. *No limit until 2012.* After December 31, 2011: 25 mg per burner

4c-II $155 \text{ W} < P \leq 405 \text{ W}$. *No limit until 2012.*
After December 31, 2011: 30 mg per burner

4c-III $P > 405 \text{ W}$. *No limit until 2012.* After December 31, 2011: 40 mg per burner

- 4d MERCURY in high pressure mercury (vapor) lamps (HPMV)
Expires on April 13, 2015
- 4e MERCURY in metal halide lamps (MH)
- 4f MERCURY in other discharge lamps for special purposes not specifically mentioned in this
Annex
- 5a LEAD in glass of cathode ray tubes
- 5b LEAD in glass of fluorescent tubes not exceeding 0.2 % by weight
- 6a LEAD as an alloying element in steel for machining purposes and in galvanized steel containing
up to 0.35 % lead by weight
- 6b LEAD as an alloying element in aluminum containing up to 0.4 % lead by weight
- 6c Copper alloy containing up to 4 % LEAD by weight
- 7a LEAD in high melting temperature type solders (lead-based alloys containing 85 % by weight
or more lead)
- 7b LEAD in solders for servers, storage and storage array systems, network infrastructure
equipment for switching, signalling, transmission, and network management for
telecommunications
- 7c-I Electrical and electronic components containing LEAD in a glass or ceramic other than
dielectric ceramic in capacitors (piezoelectronic devices) or in a glass or ceramic matrix
compound
- 7c-
II LEAD in dielectric ceramic in capacitors for a rated voltage of 125 V AC or 250 V DC or
higher
- 7c-
III LEAD in dielectric ceramic in capacitors for a rated voltage of less than 125 V AC or 250 V
DC. *Expires on January 1, 2013*
(except spare parts for EEE placed on market before Jan 1, 2013)
- 7c-
IV LEAD in PZT-based dielectric ceramic materials for capacitors being part of integrated circuits
or discrete semiconductors
new
- 8a CADMIUM and its compounds in one shot pellet type thermal cut-offs
Expired January 1, 2012
(except spare parts for EEE placed on market before Jan 1, 2012)
- 8b CADMIUM and its compounds in electrical contacts
- 9 Hexavalent CHROMIUM as an anticorrosion agent of the carbon steel cooling system in
absorption refrigerators up to 0.75 % by weight in the cooling solution
- 9b LEAD in bearing shells and bushes for refrigerant-containing compressors for heating,
ventilation, air conditioning and refrigeration (HVACR) applications

- 11a LEAD used in C-press compliant pin connector systems
Expired September 24, 2010
(except spare parts for EEE placed on market before Sept 24, 2010)
- 11b LEAD used in other than C-press compliant pin connector systems
Expires on January 1, 2013
(except spare parts for EEE placed on market before Jan 1, 2013)
- 12 LEAD as a coating material for the thermal conduction module C-ring
Expired September 24, 2010
(except spare parts for EEE placed on market before Sept 24, 2010)
- 13a LEAD in white glasses used for optical applications
- 13b CADMIUM and LEAD in filter glasses and glasses used for reflectance standards
- 14 LEAD in solders consisting of more than two elements for the connection between pins and package of microprocessors with lead content of more than 80% and less than 85% by weight.
Expired January 1, 2011
(except spare parts for EEE placed on market before Jan 1, 2011)
- 15 LEAD in solders to complete a viable electrical connection between semiconductor die and carrier within integrated circuit flip chip packages
- 16 LEAD in linear incandescent lamps with silicate coated tubes
Expires on September 1, 2013
- 17 LEAD halide as radiant agent in high intensity discharge (HID) lamps used for professional reprography applications
- 18a LEAD as activator in the fluorescent powder (1 % lead by weight or less) of discharge lamps when used as specialty lamps for diazoprinting reprography, lithography, insect traps, photochemical and curing processes containing phosphors such as SMS. *Expired January 1, 2011*
- 18b LEAD as activator in the fluorescent powder (1 % lead by weight or less) of discharge lamps when used as sun tanning lamps containing phosphors such as BSP
- 19 LEAD with PbBiSn-Hg and PbInSn-Hg in specific compositions as main amalgam and with PbSn-Hg as auxiliary amalgam in very compact energy saving lamps (ESL). *Expired June 1, 2011*
- 20 LEAD oxide in glass used for bonding front & rear substrates of flat fluorescent lamps used for liquid crystal displays (LCD). *Expired June 1, 2011*
- 21 LEAD and CADMIUM in printing inks for the application of enamels on glasses, such as borosilicate and soda lime glasses
- 23 LEAD in finishes of fine pitch components other than connectors with a pitch of 0.65 mm and less. *Expired September 24, 2010*
(except spare parts for EEE placed on market before Sept 24, 2010)
- 24 LEAD in solders for the soldering to machined through hole discoidal or planar array ceramic

multilayer capacitors

- 25 LEAD oxide in surface conduction electron emitter displays (SED) used in structural elements, notably in the seal frit and frit ring
- 26 LEAD oxide in the glass envelope of black light blue lamps
Expired June 1, 2011
- 27 LEAD alloys as solder for transducers used in high-powered loudspeakers designated to operate for several hours at acoustic power levels of 125 dB SPL and above. *Expired September 24, 2010*
- 29 LEAD bound in crystal glass as defined in *Annex I* (Categories 1, 2, 3, 4) of *Directive 69/493/EEC*
- 30 CADMIUM alloys as electrical/mechanical solder joints to electrical conductors located directly on the voice coil in transducers used in high-powered loudspeakers with sound pressure levels of 100 dB (A) and more
- 31 LEAD in soldering materials in mercury free flat fluorescent lamps (used for liquid crystal displays, design or industrial lighting)
- 32 LEAD oxide in seal frit used for making window assemblies for Argon and Krypton laser tubes
- 33 LEAD in solders for the soldering of thin copper wires of 100 µm diameter and less in power transformers
- 34 LEAD in cermet-based trimmer potentiometer elements
- 36 MERCURY used as a cathode sputtering inhibitor in DC plasma displays with a content up to 30 mg per display. *Expired July 1, 2010*
- 37 LEAD in the plating layer of high voltage diodes on the basis of a zinc borate glass body
- 38 CADMIUM and cadmium oxide in thick film pastes used on aluminum bonded beryllium oxide
- 39 CADMIUM in color converting II-VI LEDs (< 10 µg Cd per mm² of light-emitting area) for use in solid state illumination or display systems
Expires on July 1, 2014
- 40 new CADMIUM in photoresistors for analogue optocouplers applied in professional audio equipment. *Expires on Dec 31, 2013*

Appendix 2 Interconnection Levels:

Interconnection steps or links can be defined as individual interconnect levels:

- Level 0: Gate-to-gate interconnections on a monolithic semiconductor chip.
- Level 1: Packaging of semiconductor chips into assorted packages (ceramic, plastic, metal modules with feed-throughs), DIPs (dual in line), SOICs (small outline integrated circuit), chip carriers, etc. and chip-level TAB (Tape-automated bonding) interconnects the chip to the lead frames.
- Level 2: Printed circuit board (PCB), level of interconnections. Etched metal conductor traces connect electronic device leads to PCBs and to the electrical edge connectors for off-the-board interconnection.
- Level 3: Connections between PCBs, including PCB to PCB interconnections or PCB card to “motherboard” interconnections.
- Level 4: Connections between two subassemblies: one assembled electronic module to another assembled electronic module.
- Level 5: Connections between physically separate systems via cables such as an auxiliary device to a machine interface; computer to a printer or to a monitor.

However, no longer can industry be ‘level selective’ as emerging systems are demanding a combination of multiple levels of interconnection in the same module or package unit.

A number of the solderless processes have been developed for early adoption in levels Zero and level 1 only. Others may be applicable to the higher levels. The overall assessment of these for each process is detailed in the summary worksheets.

Annex B ~ Sintered Silver Literature Review

There is an ongoing search in the microelectronics packaging industry for reliable and environmentally friendly interconnect materials. Due to Restrictions of Hazardous Substances (RoHS) directives, manufacturers face the challenge of finding alternatives to lead-based solders for high temperature applications. There is also an increase in the use of power semiconductor devices such as silicon carbide and gallium nitride which need interconnect materials to operate at high switching speeds, high current densities and junction temperatures of more than 200°C [1-6]. Traditional packaging materials would not work in this harsh environment. One possible candidate to replace traditional materials and interconnect methods is the use of sintering.

Sintering is a method for making solid objects from a powder. The powder is heated in a furnace until the powder particles adhere to each other by solid state diffusion. This process occurs at a temperature well below the melting point of the material, and is therefore quite different to the solder process which relies on the melting and solidification of solder alloys.

The use of sintered silver should provide good thermal, electrical and mechanical properties and a high-temperature capability for interconnect solutions. The low thermal resistance of sintered silver also makes this interconnect method suitable for die-bonding light-emitting diodes (LEDs) [6-8]. Silver has a melting point of 961°C but sinter temperatures of less than 275°C have been achieved when using nanoscale powders [9-14]. The nano powders are typically between 20 nm and 50 nm in size [3, 11, 12, 15-17]. The use of nano particles is related to the science of sintering. The driving force for the densification increases with decreasing particle size [12] hence using nanoparticles as opposed to micro-particles decreases the effective sintering temperature. The extent of densification depends on factors such as uniformity of dispersion, particle size and particle size distribution, temperature, heating time, effect of surrounding dies/substrates. These parameters have a significant effect on the green (un-sintered) microstructure which in turn influences the final sintered structure [14]. Densification occurs by solid-state diffusion processes that are much slower than straight melting, such as in the solder process [14].

Much of the literature is focussed on the use of nano silver particles that have been formed into a paste [1-3, 5, 6, 8-10, 12-23] rather than raw powder [11]. The silver nano particles are combined with capping agents/dispersants, binders and solvents. The dispersant helps prevent the particles from agglomerating, a major issue with nano sized particles, by passivating the particles. The binders and solvents give the paste the necessary consistency to provide the green strength to the dried paste while allowing the paste to be printable [14]. These added components are detrimental to the sinter process [17]. A typical sinter profile includes a drying stage to remove the solvents and organics prior to densification [1, 2, 14, 17] with some researchers suggesting multiple drying steps [5, 14]. The standard procedure is to place the component on the paste prior to the drying stage, although Bajwa et al [4] found that printing, drying then placing the component before sintering worked better in terms of shear strength. It was suggested that this is due to bubbles appearing in the paste as organics are burnt off, that cannot escape from under the component. When drying the paste with large components in place it is also possible that not enough oxygen can reach the centre of the paste to burn off the organics in this region, resulting in a paste that won't sinter well under the centre of the component [24]. Silver nano particles will self-sinter without the application of any pressure if their capping agents are removed; however a minimum pressure (threshold stress) must be exceeded to form a reliable sintered silver joint [2]. It is not necessary to completely remove the capping agent to obtain good sintering, but organic residues may affect long-term reliability [2]. Because of the inherent instability of the nano particles, it is necessary that the desired sinter temperature is reached by the time the organic molecules are burnt off [14].

New methods of nano particle preparation have also been developed that produce pastes which don't require pressure on sintering. These pastes are prepared with a much reduced organic component. Examples include the use of Metallo-Organic (MO) technology to minimise the coating material [6]

and the deposition of nanoscale layers of polyvinylpyrrolidone [17]. Heating on air decomposes the organic compounds and the paste will sinter without any applied pressure at temperatures between 200 °C and 300 °C.

Silver nano particle pastes are particularly suited to sintering due to their reactivity and therefore propensity to sinter, but along with the need to passivate the particles and to add organic components to prevent agglomeration, the high cost of nano particles can inhibit their use in larger-scale manufacturing [7, 24]. An alternative route is to use lower-cost micron sized silver particles. Recent developments have shown this is a viable option. One approach is to use 'endothermically decomposable silver' compounds such as silver oxide or silver lactate, that will form silver particles when heated to approximately 230 °C to 350 °C to bridge the silver fillers in the micron-silver paste. Silver oxides are thermally unstable and they can easily reduce to metallic silver at these temperatures to allow sintering to occur [2, 24, 25]. In the presence of oxygen silver atoms diffuse to neighbouring atoms at temperatures as low as 184 °C for the initiation of sintering. Instead of applying pressure, it is possible to use a silver paste containing a high weight percent (e.g. 92 wt%) silver particles to produce sintered silver joints during pressureless sintering. Due to the high weight percent of silver particles, solvent must be used to control paste viscosity and also to reduce the substrate oxides so that sintering can occur [2, 7].

Some material suppliers are developing low-pressure sintered silver paste. Typical formulations have a mixture of nano and micron sized particles and need a lower volume of capping agents/dispersants in the paste, leading to fewer voids and higher reliability after joint formation. With these pastes a threshold stress (as low as 0.007 – 0.4 MPa) must be exceeded to achieve a significant increase in the density and strength of the joint [2].

As noted above, sintering does not progress in the absence of oxygen [7, 16, 25]. Sintering in inert atmospheres is much slower. Results show that sintering in air while a large chip covers the silver layer severely constrains the diffusion path for oxygen and hence results in much slower sintering, closer to sintering in nitrogen [16]. If an increase in pressure is applied the effect is more than compensated for, leading to faster sintering.

Nano and micron-sized silver pastes are designed to be printable using standard methods. Due to particle sizes it is easier to produce thicker printed layers with micron-sized silver particle pastes. Single, thick layers of nano sized pastes are prone to crack formation [24]. Both sintered pastes are suitable for a double printing method to increase the bond line thickness [4, 21, 22]. The procedure is to print a layer of paste, dry, print another layer on top, place component and then dry again before sintering. Drying the first layer must be done slowly to prevent cracking. Once a silver paste has been sintered it will not melt unless it is heated to 961°C. This means that the paste can be used for subsequent die attachments as well as other interconnections in a process that involves multiple joining steps [14, 20].

Obtaining a reliable silver joint is a balance between sinter time, sinter temperature and applied pressure. Solid-state sintering by its very nature is a relatively slow process and depends on temperature-activated diffusion mechanisms [21]. To achieve lower temperature sintering one strategy is to use applied pressure to increase the sintering driving force [1]. The application of pressure is also known to decrease porosity and increase adherence [5]. Bonding quality increases with each factor (increased time, temperature, pressure) but with no strong interaction between any two factors [21]. If both temperature and pressure are reduced, the sinter time generally needs to increase. For a given sinter time and temperature, increasing the pressure increases the shear strength of the sintered joint up to a certain point, where application of increased pressure does not increase strength any further [4]. Larger pressures are required for larger chips to sinter the paste properly underneath the centre of the chip [16].

A requirement for large pressures complicates the manufacturing process and places critical demands on substrate flatness and chip thickness [12]. Pressure must be applied directly to the components,

which can cause damage and high scrap rates [16]. Special pressure-sintering equipment is needed, and the press platen that comes into contact with the components is typically cushioned using high-temperature rubber such as silicone rubber [2, 16]. Pressing at temperatures above 200 °C can cause significant wear and tear on the processing equipment, particularly on the cushioning material, resulting in high maintenance costs [21]. It has been suggested that applying pressure to the paste during the drying stage rather than the sinter stage is an alternative way to reduce wear and tear on the presses and cushioning material used [21]. Applying pressure during the drying time results in a dense sintered material with few voids. The application of pressure is beneficial to the double print method. In this method, the second layer applied is thin and is constrained by the first layer and the component and is therefore susceptible to cracking due to constrained drying. Application of pressure mitigates this effect and increases the dried density [21].

The use of pressureless sinter paste removes the need for heated presses, although it is not unusual in industry to apply pressure during the sintering of pressureless silver paste to control density and reliability of the sintered silver joint [2, 17, 20].

Along with sinter temperature, time and pressure, the reliability of sintered silver joints also depends on other factors such as selection of metallization or plating schemes, types of substrate and substrate roughness. It has been demonstrated that surface roughness has an influence on joint shear strength when pressureless sintering methods are used (increased surface roughness leads to a decrease in strength). Applying pressure during sintering seems to overcome the surface roughness effect, with comparable joint strengths obtained irrespective of surface roughness [5].

Sintered silver pastes readily sinter onto silver surfaces and other noble metals such as gold, platinum, palladium. It is more difficult to sinter to bare copper, hence metallization or plating of the substrate surface is usually undertaken [2]. Examples are silver plated copper [1, 5, 21, 25], gold plated copper [5], Ni/Ag [1], Ni/Au, Ti/Ag [4], Ti/Ni/Ag [4, 20] and Ni/P/Au [24] metallization on copper. The nickel layer acts as a diffusion barrier layer to prevent silver/copper diffusion, while silver or gold are used to enhance bonding to the sintered silver. When bare copper was used, cleaning and etching were recommended [4, 5].

Another important aspect is the metallization of the component. Examples of this include Ti/Ni/Au, Ti/Ag, Ti/Au [4] and Ni/Ag [24] metallization on chips and Ti/Ni/Ag coated silicon die [25]. Silver and gold are suitable for the sintering process, Ni acts as a diffusion barrier and Ti acts as the seed layer.

Microstructural analyses of sintered silver joints have generally shown homogeneous cross sections with regular thickness [20]. Different porosity levels are found between pastes from different manufacturers [25]. Poor dispensing/dispersal leads to increased voids [25]. Microstructural observations have also shown that when creating a sintered silver joint, more porosity occurs due to the constrained sintering effect which prevents the sintered material from shrinking between dies and substrates [1] and indeed the sintering microstructure achieved under a large chip is different to the uncovered sintered case [16]. Metal shrinkage is also a possible cause of separation at the edge of the component [25]. After thermal cycling with a maximum temperature of 255 °C, microscopic examination revealed many cracks and defects and it is thought that CTE mismatch may be a factor in the growth of these cracks [5].

Silver sintering is accepted as a high reliability technology with promising properties such as high shear strength, high electrical and thermal conductivity and long lifetimes at high temperatures [8, 20, 22, 24]. The electrical and thermal conductivity of the low temperature sintered silver is about 3-5 times those of the best solders and much higher than that of conductive epoxies [14]. Improved electrical conductivity gives great current handling capability and excellent electrical performance, while higher thermal conductivity results in a lower junction temperature at a given level of current density. The uniformity of a silver joint eliminates the possibility of hot spots in power devices resulting in superior thermal management capability [8, 12, 14, 15, 19]. Electrical testing has shown

that porosity and cracking could be detrimental to the joint resistance and that shear strength does not provide a good prediction of electrical properties [25].

In terms of ageing, sintered silver gives much higher shear strengths after ageing than solders whose mechanical stability decreases with storage time [23]. At ageing temperatures of around 200 °C there was found to be an initial increase in shear strength with time up to a maximum value, where it then levelled off. At an ageing temperature of 250 °C no increase in shear strength with time was observed [3]. With increased ageing time, the microstructure of the sintered joint changes towards a coarse structure with large silver grains but also large pores [3].

Sintered silver joints initially have better thermal fatigue properties than lead and lead-free solder joints [2] but in some tests sintered materials degraded more rapidly than other interconnect materials tested at a maximum cycling temperature of 275 °C [5]. Low cycle fatigue tests on single lap shear joints at room temperature show stable shear stresses until sudden fracturing. This behaviour is explained as microcracks forming along grain boundaries or within grains. Once the density of cracks reaches a percolation threshold the cracks form a large cluster and become unstable [23]. Low cycle fatigue tests at 325 °C show an obvious peak in shear stress before joint failure. At this temperature the microcracks, once initiated, propagate rapidly causing a gradual decline in shear strength [23]. The peak shear stress bearing capacity and fatigue life of a joint both decrease with rise in temperature [23]. It is suggested that a sintered silver joint has good thermal-fatigue properties if its density is sufficiently high to resist fatigue fracture but low enough for stress relief [2].

The sintered porous silver has an apparent elastic modulus which is substantially lower than that of bulk silver, as well as most solder materials, as expected from its structure. The lower elastic modulus of the porous silver may be beneficial in achieving a more reliable joint between the device and substrate because of increased compliance that can better accommodate stress arising from thermal expansion mismatch [26]. Unlike low-temperature soldering techniques, bonds formed by sintering have been proved to withstand temperatures above the bonding temperature [13].

Degradation of shear strength during thermal cycling is due to the fragility of the porous sintered structure. To improve this, resin reinforcing technology has been developed. By adding special resin to the pastes, the porous area is filled with resin and the sintered structure is reinforced [6, 27]. Typical cure profiles range from 200 °C for 60 minutes [6] to 175 °C for 30 minutes [27] and the systems are designed so that the silver sinters before the resin cures. These sinter adhesives are shown to outperform conventional isotropic conductive adhesives for thermal conductivity and electrical resistance [6, 27] with no degradation in shear strength after thermal cycling up to 1000 cycles. It is possible though, that epoxy degradation could lead to cracking of the sintered silver joints during ageing [2]. It is not known whether the polymer also improves adhesion to the substrate. This method is different to that of the conductive adhesives where only minimum amounts of silver powder/flake are incorporated into the resin to create electrical pathways [26].

1. WANG, T., CHEN, X., LU, G-Q. and LEI, G-Y, "Low-Temperature Sintering with Nano-Silver Paste in Die-Attached Interconnection", J. Electronic Materials, V36, No. 10, 1333-1340, 2007
2. SIOW, K.S, "Are Sintered Silver Joints Ready for Use as Interconnect Material in Microelectronic Packaging?" ", J. Electronic Materials, 1-15, 2014
3. EGELKRAUT, S., FREY, L., KNOERR, M. and SCHLETZ, A., "Evolution of shear strength and microstructure of die bonding technologies for high temperature applications during thermal aging", 12th Electronics Packaging Technology Conference (EPTC 2010), 660-667, 2010
4. BAJWA, A. A., ZEISER, R. and WILDE, J., "Process optimization and characterization of a novel micro-scaled silver sintering paste as a die-attach material for high temperature high power semiconductor devices", Proceedings of the 36th International Spring Seminar on Electronics Technology (ISSE), 53-58, 2013

5. NAVARRO, L. A., PERPINA, X., GODIGNON, P., MONTSERRAT, J., BANU, V., VELLVEHI, M. and JORDA, X., "Thermomechanical Assessment of Die-Attach Materials for Wide Bandgap Semiconductor Devices and Harsh Environment Applications", IEEE Transactions on Power Electronics, V29, 5, 2261-2271, 2014
6. SASAKI, K. and MIZUMURA, N., "Development of low temperature sintered nano silver pastes using MO technology and resin reinforcing technology", IEEE 63rd Electronic Components and Technology Conference, 1066-1070, 2013
7. KURAMOTO, M., OGAWA, S., NIWA, M., KIM, K-S. and SUGANUMA, K., "Die Bonding for a Nitride Light-Emitting Diode by Low-Temperature Sintering of Micrometer Size Silver Particles", IEEE Transactions on Components and Packaging Technologies, V33, 4, 801-808, 2010
8. PANACCIONE, P., WANG, T., CHEN, X., LUO, S. and LU, G-Q., "Improved Heat Dissipation and Optical Performance of High-power LED Packaging with Sintered Nanosilver Die-attach Material", 6th International Conference and Exhibition on Device Packaging, Arizona, USA, March 9-11, 2010
9. LEI, T. G., CALATA, J. N., LU, G-Q., CHEN, X. and LUO, S., "Low-Temperature Sintering of Nanoscale Silver Paste for Attaching Large-Area (>100 mm²) Chips" IEEE Transactions on Components and Packaging Technologies, 33, 98-104, 2010
10. LU, G-Q., CALATA, J. N., LEI, T. G. and CHEN, X., "Low-temperature and pressureless sintering technology for high-performance and high- temperature interconnection of semiconductor devices" 2007 International Conference on Thermal, Mechanical and Multi-Physics Simulation Experiments in Microelectronics and Micro-Systems. EuroSime 2007, 698-702
11. MOON, K-S., DONG, H., MARIC, R., POTHUKUCHI, S., HUNT, A., LI, Y. and WONG, C. P., "Thermal behavior of silver nanoparticles for low-temperature interconnect applications" Journal of Electronic Materials, 34, 168-175, 2005
12. LU, G-Q., CALATA, J. N. and LEI, T. G., "Low-temperature sintering of nanoscale silver paste for power chip attachment" 5th International Conference on Integrated Power Electronic Systems, CIPS 2008, 113-117
13. ALARIFI, H., HU, A., YAVUZ, M. and ZHOU, Y. N., "Silver Nanoparticle Paste for Low-temperature Bonding of Copper" Journal of Electronic Materials, 40, 1394-1402, 2011
14. CALATA, J. N., LEI, T. G. and LU, G-Q., "Low Temperature Sintering of Nanosilver Paste for High-Temperature Device Interconnection" Empfasis Publication November 2006, <http://www.empf.org/empfasis/index.html>
15. BAI, J.G., ZANG, Z-Z., CALATA, J.N. and LU, G-Q., "Low-temperature sintered nanoscale silver as a novel semiconductor device-Metallized Substrate interconnect material", IEEE Transactions on Components and Packaging Technologies, 29, 589-593, 2006
16. KNOERR, M. and SCHLETZ, A., "Power Semiconductor Joining through Sintering of Silver Nanoparticles: Evaluation of Influence of Parameters Time, Temperature and Pressure on Density, Strength and Reliability", CIPS 2010, Nuremburg, Germany, March 16-18, 2010
17. YAN, J., ZOU, G., WU, A-P., REN, J., YAN, J., HU, A. and ZHOU, Y., "Pressureless bonding process using Ag nanoparticle paste for flexible electronics packaging", Scripta Materialia, 66, 582-585, 2012

18. LI, X., CHEN, X., YU, D-J. and LU, G-Q., "Study on adhesive reliability of low-temperature sintered high power LED modules", Proceedings of the 2010 11th International Conference on Electronic Packaging Technology & High Density Packaging (ICEPT-HDP 2010), 1371-1376, 2010
19. WANG, T., LEI, G., CHEN, X., GUIDO, L., NGO, K. and LU, G-Q. "Improved thermal performance of high-power LED by using low-temperature sintered chip attachment", 2009 International Conference on Electronic Packaging Technology & High Density Packaging (ICEPT-HDP 2009), 581-584, 2009
20. MASSON, A., AZZOPARDI, S., Le HENAFF, F., DELETAGE, J. Y., WOIRGARD, E., BONTEMPS, S. and JOGUET, J., "Processing and characterization of a 100% low-temperature Ag-sintered three-dimensional structure", 15th European Conference on Power Electronics and Applications (EPE), 2013
21. XIAO, K., CALATA, J. N., ZHENG, H., NGO, K. D. T. and LU, G-Q., "Simplification of the Nanosilver Sintering Process for Large-Area Semiconductor Chip Bonding: Reduction of Hot-Pressing Temperature below 200 °C", IEEE Transactions on Components, Packaging and Manufacturing Technology, 3, 8, 1271-1278, 2013
22. SABBAH, W., AZZOPARDI, S., BUTTAY, C., MEURET, R. and WOIRGARD, E., "Study of die attach technologies for high temperature power electronics: Silver sintering and gold-germanium alloy", Microelectronics Reliability, 53, 9-11, 1617-1621, 2013
23. LI, X., CHEN, X and LU, G-Q, "Isothermal low cycle fatigue behavior of nano-silver sintered single lap shear joint", Proceedings of the 13th International Conference on Electronic Packaging Technology & High Density Packaging (ICEPT-HDP), 1209-1215, 2012
24. SCHMITT, W., "New silver contact pastes from high pressure sintering to low pressure sintering", 3rd Electronic System-Integration Technology Conference (ESTC 2010), 2010
25. SIOW, K. S., "Sintered silver (Ag) as lead-free die attach materials", 35th IEEE/CPMT International Electronics Manufacturing Technology Conference (IEMT 2012), 2012
26. YIM, M.J., LI, Y., MOON, K-S., PAIK, K.W. and WONG, C. P. "Review of recent advances in electrically conductive adhesive materials and technologies in electronic packaging", Journal of Adhesion Science and Technology, 22, 1593-1630, 2008
27. LOWER, Y., KREBS, T. and THOMAS, M., "Sinter adhesive - new horizons in semiconductor packaging", IEEE 13th Electronics Packaging Technology Conference (EPTC 2011), 88-92, 2011