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The Influence of Solderability on Reliability in Electronic Assemblies

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ABSTRACT

The impact of solderability degradation on solder joint fatigue is discussed and exemplary data on ceramic chip resistors are given. Components were exposed, prior to assembly, to six ageing regimes to modify the solderability of the surface finish. Following the accelerated ageing for various times at 155°C, components were assembled using no-clean reflow soldering. The solder fillets on these components ranged from unacceptable non-wetting to excellent wetting. The process yield was correlated with the solderability. Assemblies were then thermally cycled between -20 and 100°C. The results revealed that the thermal fatigue failure rate, as measured by electrical continuity of the resistors, is correlated with solderability. The relationship between solderability and solder fillet shape, and hence process yield, has been demonstrated, and in turn solderability and yield has been correlated with thermal fatigue properties.

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1 INTRODUCTION

Predictions of products' lifetimes are often required and are clearly more important for safety critical and military applications, than in most domestic scenarios. For the majority of surface mount (SM) products the most common cause of mechanical stress is caused by mismatches in thermal coefficients of expansions (TCE) of the various PCB assembly components. As assemblies are cycled between the power on and off state, in different ambient temperature states, all the components experience varying degrees of physical stress depending on their size and relative TCE mismatch. The energy created in this stress cycling is absorbed by the component, the component lead, the solder fillet and the substrate. In most instances this energy is principally absorbed in the component lead and the solder fillet, but when there is no component lead, such as for LCCCs, chip capacitors and resistors, the energy is lost largely within the joint. Hence thermal cycling is far more severe for LCCCs, chip capacitors and resistors than for leaded components, which benefit significantly from the compliance conferred by the lead. The relative TCE values for a resistor assembly are shown in Figure 1. As can be seen the largest difference in TCE is between the ceramic resistor body and the solder, but the biggest strain will result from the difference between ceramic and the substrate since this is operating over a larger distance.

To screen products from failing by stresses resulting from temperature excursions, complete PCBs are thermally cycled in chambers to test their reliability, and the results from the test used to qualify the design and production process. This however assumes a future product is the same or better than our original test pieces. What if the solderability of the current batch of 0805 capacitors is marginal? Clearly if the solderability is poor, the wetting will be poor, and solder will not rise so far up the component lead and a different fillet shape will be formed. We would clearly expect the poorer joint to fail earlier, but the relation between fillet shape and time to failure and hence reliability is not known. It is precisely this area that we address here.

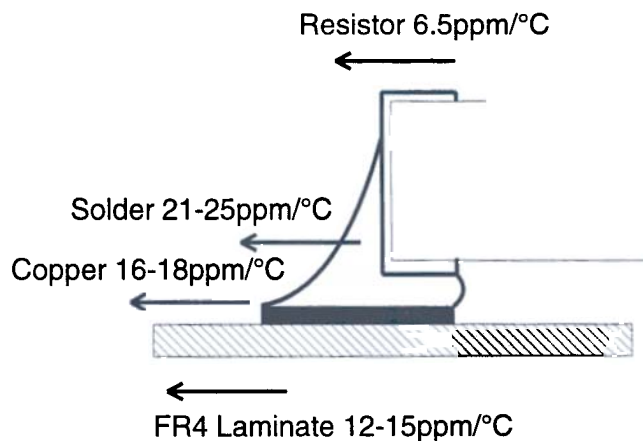


Figure 1: TCE (x-axis) mismatches in SM assemblies

Thermal cycling of PCB assemblies is an accelerated test which aims to replicate the stresses experienced in service. To accelerate the time to failure the testing conditions are often more extreme than the product would normally be exposed to, in terms of temperature limits and the rate of temperature change. However caution must be exercised in using these accelerated conditions to ensure that failure modes in the test are the same as those encountered by the product in normal use. There are few standards in this area and most testing is done to in-house

standards. The NPL surveyed companies in the UK and produced the results in Figure 2. These show a wide range, and reflect the application, which varies from military to domestic.

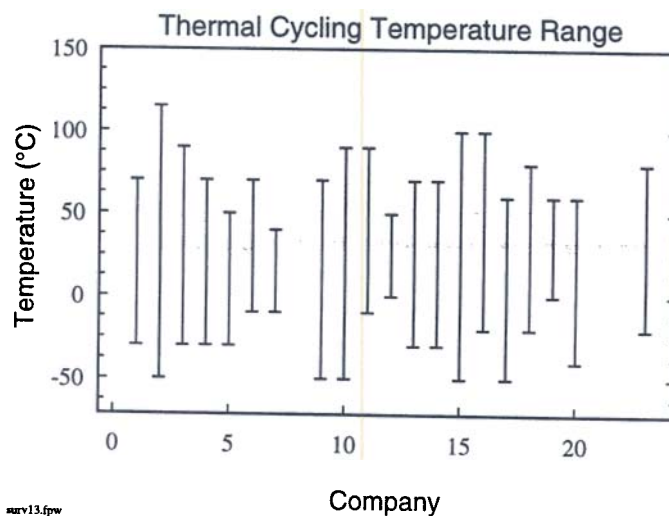


Figure 2: Results of a survey of thermal cycling conditions used by UK companies.

2 EXPERIMENTAL

Manufacture of Test Assemblies

For this study sixty PCB assemblies were manufactured by a contract manufacturer with SM capability. Each assembly incorporated fifty 0805 chip resistors (1000Ω). The resistors were arranged in independent circuits on the PCB and could be electrically monitored individually using a multiple pole switching system and a digital volt meter via a 50 way connector. During thermal cycling, this circuit design enabled the majority of resistors on each assembly to be monitored periodically at room temperature and a selection of resistors to be monitored during thermal cycling at both the hot and cold dwells in the cycle. The value of all resistors soldered to the assembly was checked electrically after assembly using this method. The layout of the assembly is shown in Figure 3. The design also incorporates three SOIC14s (1.27mm pitch (0.050 inches) and one QFP120 (1mm pitch (0.040 inches)). These devices could not be monitored electrically. The PCB was a double-sided FR4 substrate, 1mm(0.040 inches) thick, with a photo-imageable wet solder resist. All PCBs were from the same batch from a single manufacturer.

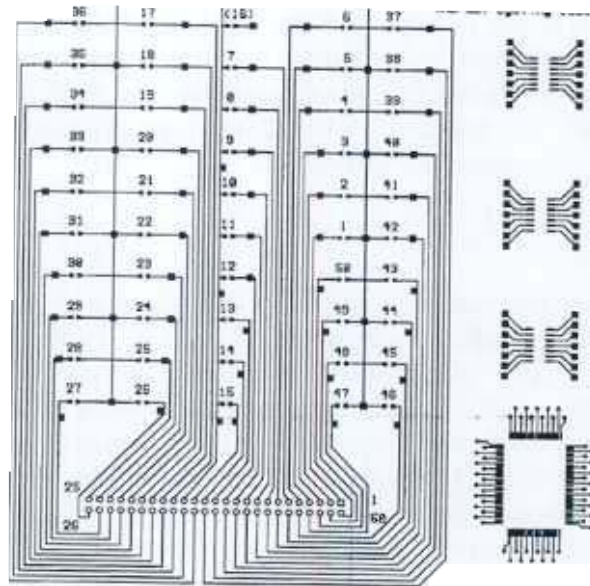


Figure 3: Layout of test assembly

The resistors used were all from a single reel of components from a major European manufacturer. The terminations were of the nickel barrier type with a plating of 90Sn10Pb to an average thickness of 9.4 μm . To investigate the effects of varying solderability, a number of components were artificially aged in an air-circulation oven at 155°C as described in the IEC 68-2 series of standards. Previous work at the National Physical Laboratory has shown this ageing method to be very repeatable (Ref. 1). The ageing regime is given in Table 1. The assembly process and constituent parts were identical for all assemblies with the exception of the solderability of the surface mount resistors.

Table 1: Artificial Ageing Regime for Resistors at 155°C

Heat Treatment Designation	Age 1	Age 2	Age 3	Age 4	Age 5	Age 6
Hours at 155°C	0	50	150	300	700	1000

The solderability of the resistor terminations after ageing was determined using a Multicore MUST System II solderability tester using the globule test method carried out to IEC 68-2-69. The solder temperature was 235°C and the solder used was 60/40 SnPb. The flux was as specified in IEC 68-2-20 with 0.5% chloride and was supplied by Multicore Solders as Actiec 5. The components were dipped at 1mm/sec to a depth of 0.1mm. The force at two seconds was tabulated for all the measurements.

The assembly method was a simple single-sided reflow process of stencil printed solder paste, placement using manual placement equipment and mixed IR/convection reflow. A single pot of paste (60/40 Sn/Pb with no-clean flux) was used. Only one operator was used for each operation. The stencil used was manufactured from 0.15mm stainless steel. Apertures were chemically etched with a 10% linear reduction on corresponding component land size. It was

not feasible to machine place the components as they had to be removed from tape to be artificially aged. All assemblies were reflow soldered using the same profile in a mixed convection/IR machine. The peak reflow temperature was 220°C and the maximum molten solder time was 45secs. No touch-up was allowed at any part of the process including post-solder. The assemblies were left uncleaned.

Visual Inspection

After manufacture every joint on each assembly was visually inspected using a stereo zoom microscope with 10-30x magnification by a single operator. Hence 6000 joints were inspected and marked. Each solder joint was given a score out of five for the height of fillet rise and a similar score for wetting angle. A diagrammatic representation of the scoring system is given in Figure 4. A wetting angle value of 2 corresponds to an approximate wetting angle of 90° and a score of 1 is greater than 90°. A fillet rise value of 2 corresponds to a fillet rise of a quarter the component height. Both these criteria are recognised in many National standards as being the minimum acceptable solder joint criteria. An unacceptable joint is considered to have a wetting angle of less than or equal to 2 and a fillet height of less than 2. Thus an ideal joint with a low wetting angle and fillet rise to the top of the component would be given a score of 10 (5+5). An unsoldered joint with no fillet rise would score a 2(1+1).

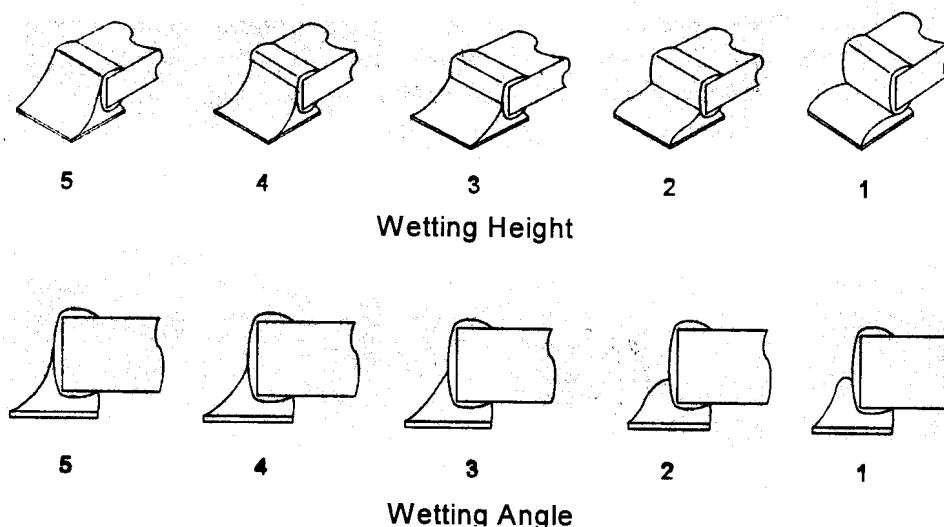


Figure 4: Fillet rise and wetting angle criteria

Despite generating more than 1500 visually defective joints, the post-assembly electrical test could only locate one component with a resistance of greater than 1050Ω. This was a tombstoned resistor which was an open circuit. All other components exhibited an electrical resistance which was within the tolerance of the resistor (1000 Ω +/- 5%). This important result confirms the widely held belief that electrical testing is not a reliable method of finding substandard solder joints.

Thermal Cycling

The assembled PCBs were then inserted into a cycling oven for thermal cycling. The cycle was selected on the basis of being representative of what is currently in use, based on what is in Figure 2, and the damage to the substrate if the T_g is exceeded. The two hold temperatures were -20 and 100°C with 30 minute dwells and 15 minute ramps between the hold temperatures. The resistance measurements taken in-situ during the cycling were taken 25 minutes after the start of the dwell.

3 RESULTS

Solderability Measurements

The solderability of lead terminations for each age of component is plotted in Figure 5. The solderability degradation follows typical ageing behaviour. There is initial deterioration due to oxidation of the fusible coating, which is a smaller effect than that due to the penetration of the intermetallic at the surface and the oxidation of that intermetallic. When the intermetallic oxide has formed on a large part of the surface, the surface is rendered completely unsolderable to electronics grade fluxes. At 1000 hours the solderability has fallen to the minimum value as measured on the wetting balance for this component.

The process yield was calculated and is shown in Figure 5 with the solderability data. The yield data was calculated as a percentage based on a total possible visual inspection score, using the criteria discussed above. Hence an average score of 9 corresponds to a 90% yield.

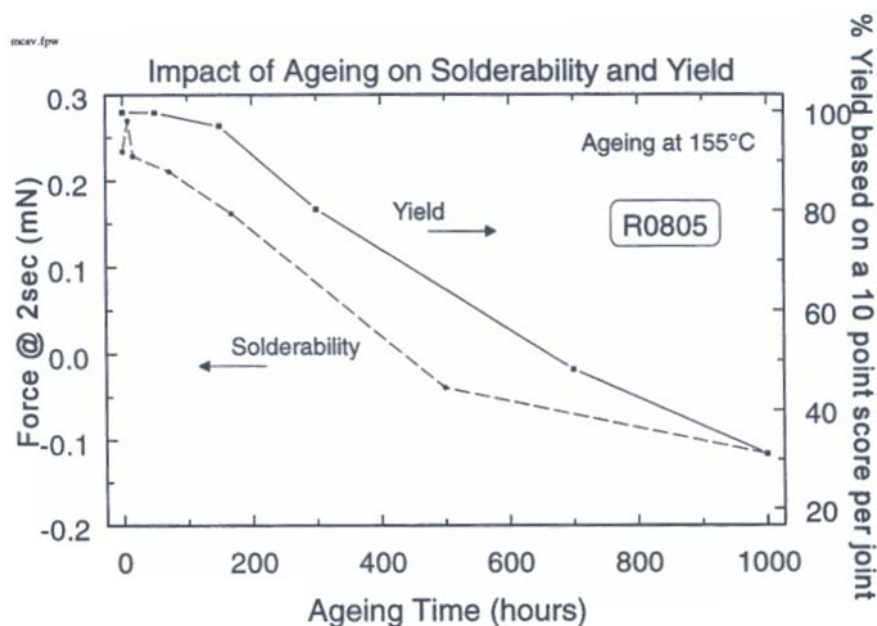


Figure 5: Comparison of solderability & process yield

It is immediately apparent from Figure 5 that there is an excellent correlation between solderability and yield. It should be noted that the axes have not been manipulated. This result demonstrates the effect of solderability, as measured with the wetting balance, on the yield. Each PCBs assembly also contained three SOICs and one QFP. Very similar solderability results were obtained for the SOICs and QFPs, again with a very good correlation between solderability and yield. Hence solderability measurements can be very useful in predicting yields.

Visual Inspection

The acceptance criteria described above were that a joint with a 2 or 1 for either wetting angle or fillet rise were unacceptable. A plot of the number of unacceptable joints for each age is shown in Figure 6. For each age conditions there are 1000 joints. Using these criteria it is clear for a sub 1000 ppm defect process the solderability must be close to the as received high

solderability condition. As the solderability of a batch of components decreases the range of solderabilities within that batch will increase. This can be seen in Figure 6, where, at 150 hours of ageing there were 11 defective joints, 11,000 ppm defect rate, yet the solderability of the average batch is still high, as shown in Figure 5.

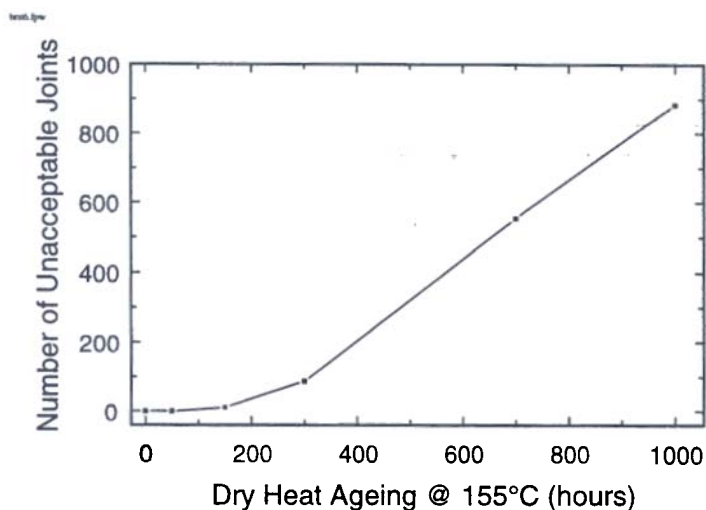


Figure 6: Effect of dry heat ageing on the total number of unacceptable joints. (Total possible number of unacceptable joints is 1000)

Thermal Cycling

Results from the thermal cycling are in three formats: periodic electrical measurements of all the resistors at room temperature; electrical measurements of 80 selected resistors during each thermal cycle, at the hot and cold holds of the cycle; and finally microsections of joints. The electrical continuity measurements taken at room temperature have been averaged for each solderability age, an average of 50 measurements for each PCB. These results are shown in Figure 7 for Age 6. To allow averaging of results, while keeping the scale compact on a linear axis, the reciprocal of resistance has been plotted, the conductivity. Hence if the resistance increases to $2k\Omega$, the conductivity drops from 10^{-3} to 0.5×10^{-3} mhos, and if the resistance goes open circuit the conductivity is zero. Therefore reducing conductivity indicates joint failure. The results show that the same basic behaviour is occurring on each PCB, and that the 10 boards together are a very good statistical sample. The average of the 10 boards from each age are shown in Figure 8. The Age 6 results in Figure 8 at 3300 cycles show that typically 60% of the resistors have failed, but 40% are still connected. This is a somewhat surprising result considering that our visual inspection data in Figure 6 shows that 90% of the joints failed visual inspection. A similar conclusion can be drawn from the Age 5 results, where only 20% of the joints have failed.

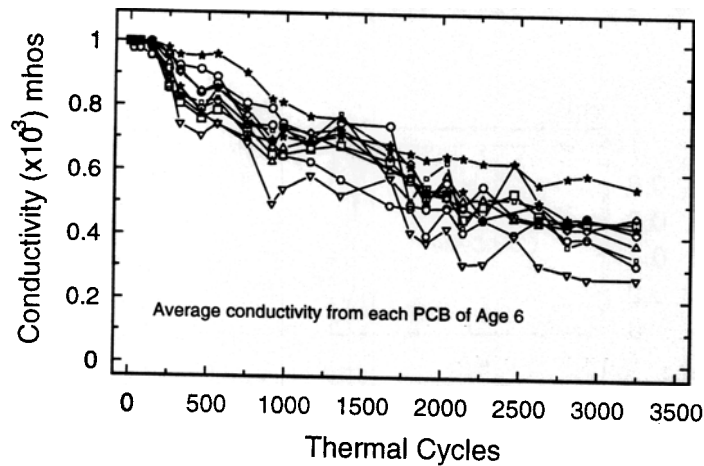


Figure 7: The average conductivity from each of 10 PCBs of 0805 resistors aged for 1000 hours at 155°C

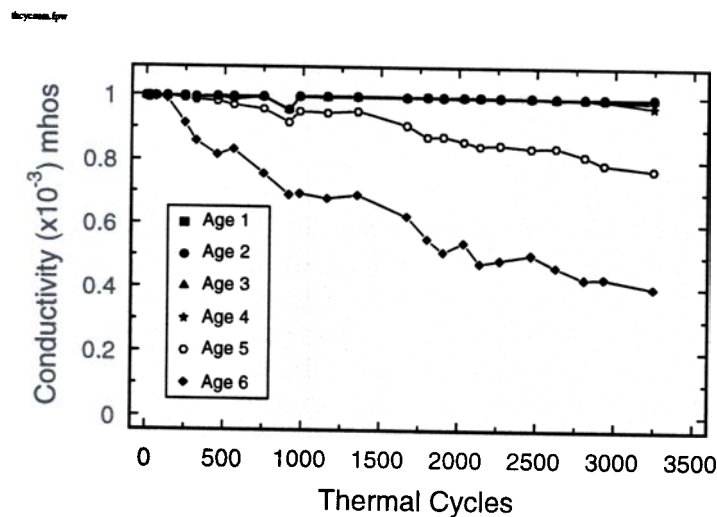


Figure 8: The average conductivity of resistors for each age

The time interval over which these measurements are taken is a significant factor in applying failure criteria. In these measurements each resistor is measured 5 times over a 1 second period, and the average recorded. Hence the values plotted in Figure 8 do represent a large degree of averaging. In many applications even small breaks in resistance for less than a microsecond will constitute failure.

As described earlier, measurements were taken from selected resistors during the thermal cycle. Results from one resistor on one of the Age 5 boards are shown in Figure 9. It is immediately clear that the resistance does not degrade gradually, but rather, fails erratically, recovering after a period of being open circuit. Also the resistor is not open circuit simultaneously for the hot and cold cycles, for the early failures before 2000 cycles. An average of all board 5 resistors show that there is no tendency for failure to occur initially in either the hot or cold cycle. Resistors may recover after going open circuit due to further movement around the crack during subsequent

thermal cycles. For a resistor in real use after the initial failure there would be no further cycling, hence the appliance would remain in a failed state.

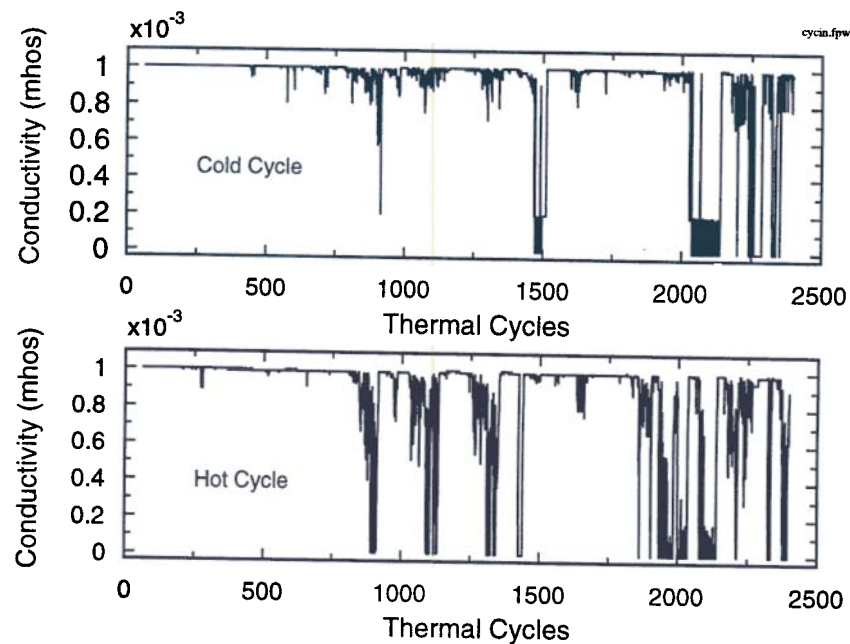


Figure 9: The conductivity values from the hot and cold cycles from one resistor, which was aged for 700 Hours at 155°C (Age 5)

Figure 10 shows microsections of various solder fillets with different visual inspection scores from thermally cycled boards, Age 5, after 2485 cycles. The thermal cycling has clearly generated cracks under all the resistors and caused grain coarsening in regions of high stress. On all the boards, Age 1 to 6 inclusive, cracking always occurs under the component. At the corner of the chip the crack tends to progress either; at an incline of 45° or follow the vertical edge of the component. It is apparent that as the fillet becomes large in front of the resistor, as in Figures 10C and 10D, the crack has further to propagate and hence the lifetime will be longer. Furthermore as the fillet detaches from the lower part of the component the remaining fillet starts to have properties similar to a lead, and hence is more compliant, further enhancing the fatigue lifetime of the component. It is pertinent to note all the components in Figure 10 were conducting when removed from the test. The boards have not experienced any vibration, which would no doubt increase the failure rate.

Microsections of the SOICs and QFPs do not show cracking up to 3000 cycles. For the leaded components the only thermal mismatch is local, between the fillet and the lead and PCB, as compared to the TCE mismatch over the device length. Further cycling and microsectioning of the joints will continue.

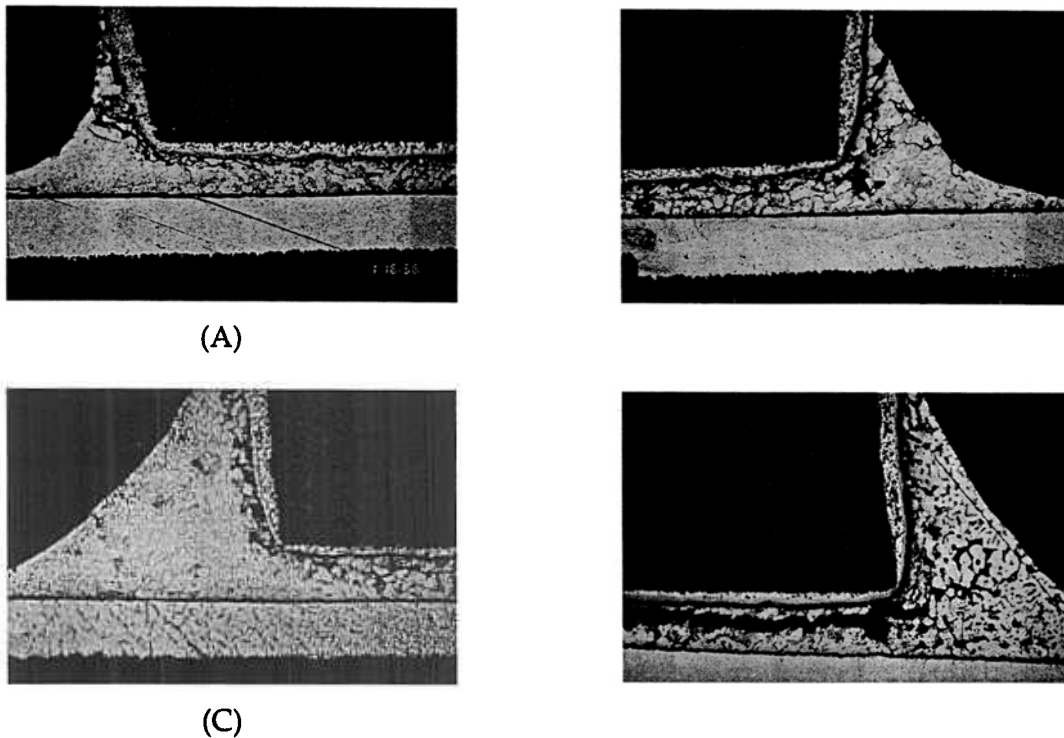


Figure 10: Microsections of joints from Age 5 boards. Fig A, B, C and D scored 3, 4, 5 and 5 respectively on the visual inspection score. The score is taken as the lower value of either the wetting angle or fillet rise score. The maximum possible score is 5. (Mag x100)

4 DISCUSSION

The work set out to correlate solderability with solder joint reliability, as measured by thermal cycling. The experiment has however produced two sets of data to correlate with solderability, one based on visual inspection and the other thermal cycling results. We will consider the visual inspection data first.

Visual inspection is recognised as subjective and open to operator error, but within this data set a high level of consistency was achieved by using the same inspector to score all the joints. These visual inspection results did show some interesting trends. The trend in process yield follows the reduction in component solderability (see Figure 5) indicating a close relationship between solderability level and process yield. Electrical testing of joint quality was completely ineffective.

Ideally an assembly process should have zero defects and therefore it is the total number of visually unacceptable joints made which some may consider to be the 'bottom line'. The nature of the process is such that a spread of measurements of fillet rises and wetting angles will be experienced. An ideal assembly process ensures that this spread is kept to a minimum and that the worst joint manufactured is still an acceptable joint. Figure 6 shows the number of visually defective solder joints for each of the dry heat component ages. These results show that unacceptable joints begin to occur sometime after 50 hours of dry heat ageing at 155°C for the process parameters used in this study. It should be noted the coating on these components is 9µm, which was the thickest in a survey of six manufacturers. This is approximately equivalent to 10 years of storage at room temperature (Ref. 2). In Figure 6 a value of 1 on the *y*-axis corresponds to a 1000 ppm defect rate. The wetting force at 2 seconds for 50 hours of ageing is

approximately 0.2 mN. This is only a 20% reduction as compared to the unaged value. This implies that if a zero defect soldering process were desired for this assembly line then components with a wetting force in excess of 0.2mN would be required. This value would vary for other assembly lines depending of the robustness of the process, flux activity, etc.

As the solderability of components decline, visual assessment of the joint quality showed changes to the joints in three areas:

- (1) solder fillet height is reduced and becomes irregular
- (2) wetting angle is increased
- (3) solder spreads over the land area away from the component giving the appearance of insufficient solder

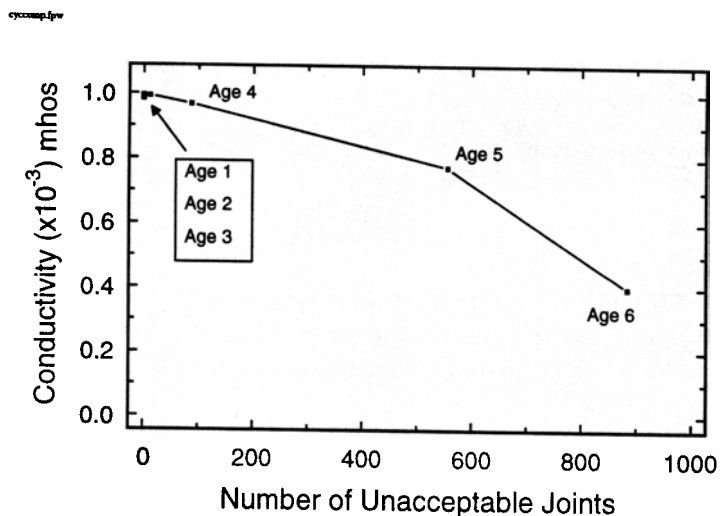


Figure 11: The correlation between visually unacceptable joints and the thermal cycling performance at 3250 cycles, as measured by electrical continuity testing, for the variously aged resistors

Thermal cycling reveals clear differences in reliability, or time to failure, between resistors with varying solderability. The thermal cycling behaviour is related to the joint shape, as the fillet rise and wetting angle become less than or equal to two, the time to failure rapidly declines. The correlation between visual inspection and reliability is shown in Figure 11. The reliability is measured as the conductivity of an average of 500 resistors for each ageing condition.

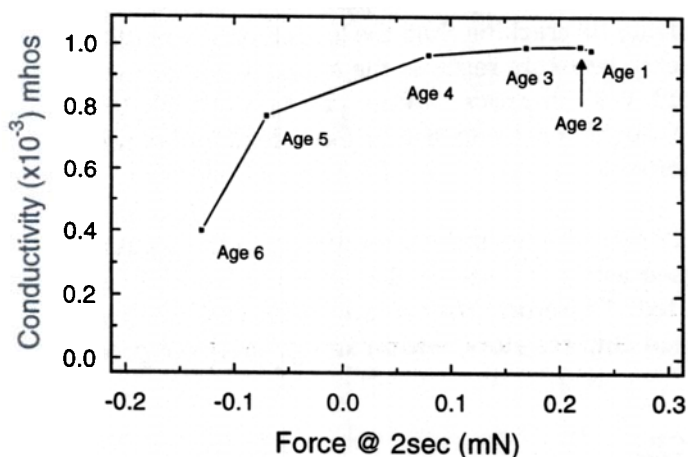


Figure 12: Correlation between solderability and the thermal cycling performance at 3250 cycles, as measured by electrical continuity testing, for the variously aged resistors

Figure 11 shows a clear correlation between joint quality and fatigue properties, and in Figure 5 the correlation between solderability and visual inspection is demonstrated. Hence a relationship between thermal fatigue cracking and solderability for these components has been established, and this is shown in Figure 12. This shows that for poor solderability the reliability is reduced, in a similar manner to the correlation for visual inspection and reliability shown in Figure 11. These data confirm the conclusion that the wetting balance measurements can be used in qualifying the future reliability of components.

The results presented here are interim, with 3250 thermal cycles completed, the experiment will continue to run until failures are observed for the Age 1 resistors, allowing the analysis to be completed.

5 CONCLUSIONS

Whilst acknowledging the qualitative nature of visual inspection, this study has highlighted several areas of interest. Process yield has been shown to be related to the solderability of components and that to obtain a zero defect process, it may be necessary to have components with solderabilities that are close to the optimum values obtainable. The solderability measurements were carried out on 10 components for each age. It is therefore clear that solderability testing is an efficient way of estimating yield prior to production.

It is pertinent to note that solderability test conditions of temperature and flux are different to those used in manufacture of the assemblies. None the less, the results demonstrate good correlation between solderability measurements and visual inspection of the joints.

Measuring joint resistance has been shown to be a poor method of attempting to find visually unacceptable joints, on all but the lowest resistor values. Certainly this was not found to be possible with 1000Ω 5% resistors.

Fatigue properties of solder joints in thermal cycling has been shown to be closely related to the fillet shape for resistors. The study has concentrated on chip resistors which have proved far more susceptible to fatigue cracking than the leaded components in the study, SOICs and QFPs. Poor fillet rise on chip resistors reduces the amount of material the crack has to penetrate to cause an open circuit. With improved wetting and greater fillet rise there is the possibility that the remaining fillet, during cracking, acting like a lead and conferring some compliance to the remaining solder joint.

The connection between fatigue and solderability, to the solder joint characteristics has been demonstrated, consequently, it is self evident that solderability and thermal fatigue properties are intimately related. Therefore, the wetting balance measurements can be used to predict reliability of soldered chip resistors, within any given set of process parameters.

6 REFERENCES

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7 ACKNOWLEDGEMENTS

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