

REPORT

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**Reliability of Electronic
Substrates After Processing
at Lead-free Soldering
Temperatures; Part 2**

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Reliability of Electronic Substrates After Processing at Lead-free Soldering Temperatures; Part 2

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ABSTRACT

European legislation has resulted in all lead-free solders now being high tin alloys with significantly higher melting points compared to the previous conventional tin-lead alloy. Reinforced resin materials, may suffer degradation caused by the associated higher processing temperatures. This is compounded by the interconnecting structures being brought into closer proximity as a result of increasing technology advances driven by miniaturisation. The removal of non-functional pads to facilitate signal routing and improved drilling conditions for high aspect ratio vias, may also affect substrate reliability.

The National Physical Laboratory and PWB Interconnect Solutions Inc. have undertaken a joint study following identical test structures through both thermal cycling, with constant electrical monitoring (event detecting) and Interconnect Stress Testing (IST). The test vehicles included patterns to monitor changes in interconnection spacing (pitch) and also the effect of removing non-functional pads. The failure modes generated with both techniques were similar as were the relative rankings of the effects. The results showed that the removal of non-functional pads tended to improve reliability for high aspect ratio plated through holes in thicker substrates, although increasing interconnection pitch had little effect on failure rate. An evaluation of different surface finishes, showed that the ENIG finished PCBs performed significantly worse than expected, which was attributed to poor nickel quality. PCBs with HASL finish performed better than those with Ag finish, due to presence of solder down the vias. PCBs of greater thickness failed earlier than thinner PCBs due to their greater z-axis expansion during soldering. Polyimide substrates consistently out-performed high Tg phenolic cured epoxy PCBs, reflecting their higher Tg.

The results generated by both thermal cycling and IST showed extremely good correlation. Failures occurred at a slightly lower number of cycles for IST compared to thermal cycling due to the more stringent failure criteria possible with IST. The relative ranking of the level of failures is identical for both the thermal cycling and IST but the results were obtained in very different timescales. IST has been shown to give fast comparable results to thermal cycle testing with constant monitoring, but thermal cycling may be more beneficial if a wider range of experimental parameters are to be tested simultaneously.

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Approved on behalf of the Managing Director, NPL,
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1 INTRODUCTION

The requirement to comply with the European regulations introduced in 2006 banning lead, has driven the adoption of new materials both in electronics assembly and bareboard manufacture. The electronics manufacturing industry has been using SnPb based solders for electrical and electronic interconnection for more than 60 years and the European ban on lead effectively discards all that experience and research into the reliability of soldered assemblies. Many organisations including NPL and PWB, are working hard to improve the knowledge and experience of lead-free reliability but many questions are still unanswered.

The alloy traditionally used for soldering in electronics manufacturing was SnPb, which has a melting point of 183°C. The replacement solders for SnPb are all high tin alloys with significantly higher melting points. The most widely used options are now tin/silver/copper alloys, which have higher melting points around 217°C, which may affect the reliability of the printed circuit substrate. As soldering temperatures are increased, the substrate will expand more in the z-axis, which increases the corresponding strain on the copper barrel of the vias with potentially increased risk of material damage.

Higher processing temperatures may also increase the propensity for multi-layer substrates to delaminate, and electrical insulation properties may be degraded, due to increased risk of dielectric breakdown by cathodic or anodic electro-migration.

These materials factors are compounded by interconnect structures being brought into closer proximity as a result of increasing technology advances driven by miniaturisation. The decision to remove non-functional pads to facilitate signal routing, reduce capacitance, increase via impedance and improve drilling conditions for fine vias, may also affect substrate reliability at lead-free soldering temperatures. The effect on reliability of removing non-functional pads has been an area of contention within the electronics industry for some time.

The work reported here forms part of a joint industry/UK government funded project to develop test methods for advanced electrical interconnect. An inter-comparison of Interconnect Stress Testing (IST) and thermal cycle testing of substrates has been undertaken, using a test vehicle to explore the effects of removing non-functional pads, reducing the spacing between vias, alternative surface finishes, variation of PCB thickness and base material of the PCB, and different conditioning of the substrates during the assembly process.

2 METHODOLOGY

2.1 TEST VEHICLE

A test panel was designed that included eight coupons of via chains, as shown in Figure 1, utilising a 10 layer structure in a high glass transition temperature (T_g), phenolic-cured glass reinforced epoxy laminate. The overall size was 230mm x 180mm. Boards were fabricated in thicknesses of 1.6, 2.5 and 3.2mm, with surface finishes of immersion Ag, ENIG (electroless nickel/immersion gold) and lead-free HASL. Additional test panels were also fabricated using glass reinforced polyimide laminate.

A single test coupon (G) was designed for thermal cycling, incorporating chains of 10:1 aspect ratio vias, on two different via grid pitches (1.0mm and 0.8mm). Some patterns included non-functional pads, whilst another had the pads removed. There was also a test pattern for μ vias.

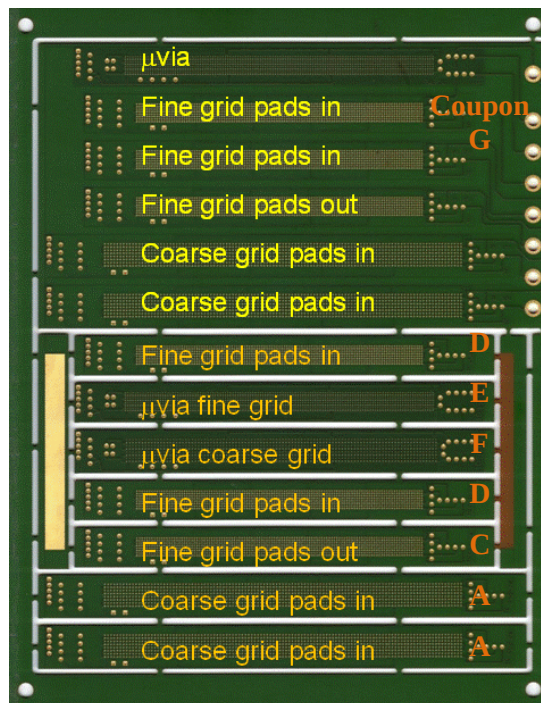


Figure 1: Test board showing individual test patterns for, at the top, thermal cycling (Coupon G), and lower down the individual IST test patterns (Coupons A, C through F)

2.2 CONDITIONING OF TEST BOARDS

To determine the worst case effects of lead-free reflow soldering on the reliability of the PCBs, test boards were conditioned using reflow soldering, wave soldering and BGA rework.

For reflow soldering, PCBs were reflowed in a BTU Pyramax 98, 7-zone reflow oven with each PCB design reaching a peak reflow temperature of 260°C, with a molten solder time of approximately 70 seconds. The boards were allowed to cool to room temperature before additional reflows were undertaken.

For wave soldering, the underside of the test boards were covered with polyimide tape to prevent solder filing any of the test vias. The wave temperature was set to 260°C.

For BGA rework conditioning a standard rework programme for a BGA403 was used. A component was fitted in place during the rework operations, inverted to prevent soldering. The routing between test circuits was closed with polyimide tape to equalise temperatures during rework. Each board was reworked in four positions as shown in Figure 2. Boards were allowed to cool to room temperature between operations. The BGA rework profile is given in Figure 3.

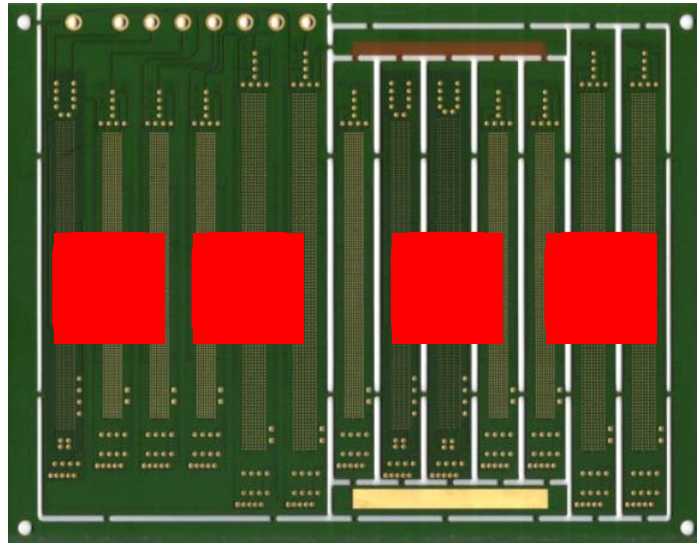


Figure 2: Position of BGA Rework Operations (rework positions shown in red)

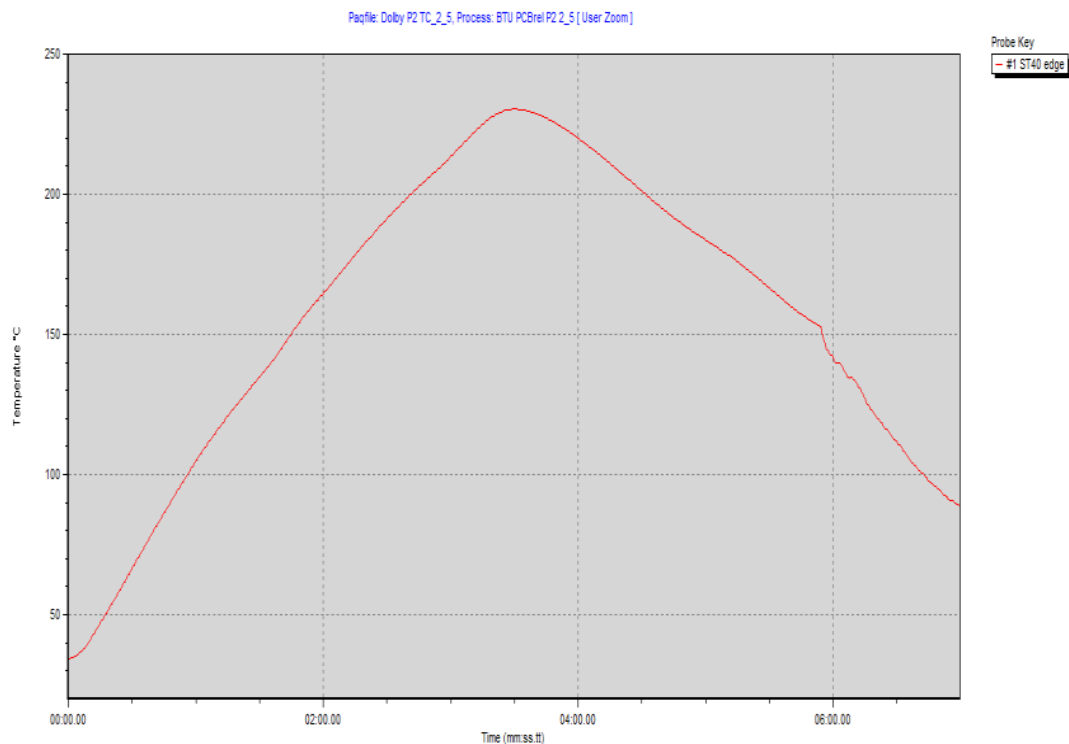


Figure 3: BGA Rework Profile

The test matrix of boards is given in Table 1.

Table 1: Test matrix

Board nos.	Surface Finish	PCB Thick.	Conditioning	Material	Testing
11-14	Ag	2.5mm	6 LF Reflows	HP	IST & T/C (-55+125)
21-24	Ag	2.5mm	6 LF Reflows	HP	IST & T/C (RT+150)
31-34	Ag	3.2mm	6 LF Reflows	HP	IST & T/C (-55+125)
41-44	Ag	1.6mm	6 LF Reflows	HP	IST & T/C (-55+125)
51-54	LF HASL	2.5mm	6 LF Reflows	HP	IST & T/C (-55+125)
61-64	Ag	2.5mm	2 X LF Wave	HP	IST & T/C (-55+125)
71-74	Ag	2.5mm	6 LF Reflows + 2 BGA Rework	HP	IST & T/C (-55+125)
81-84	Ag	2.5mm	3 LF Reflows + 2 BGA Rework	HP	IST & T/C (-55+125)
91-94	Ag	2.5mm	6 LF Reflows	Polyimide	IST & T/C (-55+125)
101-104	ENIG	2.5mm	6 LF Reflows	Polyimide	IST & T/C (-55+125)
111-114	ENIG	2.5mm	6 LF Reflows	HP	IST & T/C (-55+125)

Note: LF = lead free, HP = High Tg phenolic cured epoxy glass, T/C = thermal cycling, IST = interconnect stress testing

2.3 THERMAL CYCLING AND ELECTRICAL TEST

Thermal cycling was undertaken on coupon G. The chains of through vias and μ vias on this coupon were connected to event detectors so that the resistance of the chains could be constantly monitored. The event detectors registered a failure when the resistance of the via chain increased to $> 5k\Omega$ for a period greater than 200ns. Thermal cycling was conducted in a single chamber system up to 3000 cycles, -55°C to 125°C with 5 minute dwells and ramps of 10°C per minute, giving a total cycle time of ~ 1 hour.

2.4 INTERCONNECT STRESS TESTING

The IST was undertaken at PWB Interconnect Solutions Inc. and followed IPC TM650 standard methodology (Reference 3). This testing utilised coupons A, C and D of the test panel, with each test vehicle consisting of two independent test circuits. The first or “sense” circuit, was constructed to measure the reliability of plated through holes (PTH) barrel. The second or “power” circuit, consists of internal interconnections between the copper foils and the upper/lower layers of the PTH barrels. The power circuit is also used to homogenously heat the coupon, by passing DC current through specifically designed circuits in the outer layers, which match the heating conditions created during component assembly and product operation. Throughout IST testing both circuits are continually monitored until a preset level of electrical degradation (structural damage) is achieved, at which point the temperature cycling for each individual coupon is suspended. For this study, IST testing was performed by heating coupons from ambient to 150°C in three minutes $\pm 0/- 5$ seconds followed by cooling to ambient. Testing

continues until a circuit demonstrated a 10% increase in resistance or end of test at 2000 cycles (8 days).

2.5 COPPER THICKNESS MEASUREMENT

To ensure that comparisons could be made between PCBs manufactured in different batches, the copper thickness of example micro-sections were measured after thermal cycling. Measurements were undertaken on a Nikon MM60 measuring microscope. Measurements are an average of at least 16 measurements on two different vias.

2.6 DYNAMIC MECHANICAL ANALYSIS (DMA) OF TG

DMA measurements were undertaken on a TA Instruments DMA 2980 according to IPC-TM-650 2.4.24.2 (Reference 7) in single cantilever bending mode. The heating rate was 3°C/min with the tests being conducted on as manufactured material (i.e. before profiling). The inflection point in the storage modulus curve is the preferred point for Tg analysis (Reference 8).

2.7 THERMO-MECHANICAL ANALYSIS (TMA) OF THERMAL EXPANSION COEFFICIENTS

TMA measurements were undertaken on a TA Instruments Q400-EM system using a penetration probe (Reference 9). The materials were tested as-received and the specimens were subjected to heating and cooling cycles at 2 °C per minute and a force of 0.02N between 30 and 240 °C.

3 RESULTS AND DISCUSSION

3.1 EFFECT OF VIA WALL THICKNESS

The copper thickness measurements for the test substrates are given in **Table 2**. Ag (1) and Ag (2) refers to samples subjected to different thermal cycling regimes.

Table 2: Via copper thickness measurements

Surface Finish	PCB Thickness (mm)	Conditioning	Material	Average Cu Thickness (mm)	Minimum Cu Thickness (mm)
Ag (1)	2.5	6 LF Reflows	HP	0.024	0.016
Ag (2)	2.5	6 LF Reflows	HP	0.032	0.023
Ag	3.2	6 LF Reflows	HP	0.020	0.016
LF HASL	2.5	6 LF Reflows	HP	.025	0.019
Ag	2.5	6 LF Reflows + 2BGA Rework	HP	0.032	0.026
Ag	2.5	3 LF Reflows + 2BGA Rework	HP	0.034	0.026
Ag	2.5	6 LF Reflows	Polyimide	0.022	0.015
ENIG	2.5	6 LF Reflows	HP	0.023	0.017
Ag	1.8	6 LF Reflows	HP	0.025	0.015

3.1.1 Via wall thickness discussion

As can be seen from **Table 2**, the copper thickness of the via walls varied considerably between the test PCBs. This restricted the number of direct comparisons that could be made from the available data. IPC 6012 (Reference 5) calls for a minimum average thickness for class 3 high reliability electronic products PCBs of 0.025mm and a minimum of 0.020mm. On this basis the majority of the test substrates would have failed this criteria. Indeed approximately half the substrates would have failed the criteria for class 2 dedicated service electronics products PCBs (average = 0.020mm, minimum = 0.018mm). Whilst the via wall thicknesses vary considerably within the data set, comparisons can be made where samples have similar wall thicknesses i.e. Ag x 6LF reflows, LF HASL x 6LF reflows and ENIG which have average wall thicknesses of 0.023 to 0.025mm. Similarly where variations occur within a test panel, wall thicknesses will be the same (i.e. fine/coarse pitch grids, non-functional pads included/excluded).

3.2 EFFECT OF THE PRESENCE OF NON-FUNCTIONAL PADS

As the each test substrate incorporated test structures for both the inclusion and exclusion of non-functional pads (as shown in Figure 4), variances in the via wall thickness are not relevant and a direct comparison of results can be undertaken. The failures that were generated during thermal cycling for samples where non-functional pads were included or omitted, are shown in Figure 5, as a Weibull plot. The plot shows similar gradients for both sample sets but where non-functional pads were removed, the time to failure is greater than that for samples with the non-functional pads included. The number of cycles to 50% failures is around 700 thermal cycles when the non-functional pads included, compared to around 930 thermal cycles when the non-functional pads are removed.



Figure 4: Micro-sections of thermally cycled vias showing non-functional pads excluded (left) and included (right)

The failures that were generated for similar samples during IST testing are shown in Figure 6 as a Weibull plot. These results mirror the thermal cycling results with the plot showing similar gradients for both sample sets. Where non-functional pads have been removed, the time to failure is greater than that for samples with the non-functional pads included. A comparison is detailed in Table 3.

Table 3: Comparison on the effect of including or removing non-functional pads on IST failures

	Number of cycles to 50% IST failures
Non-functional pads included	550
Non-functional pads removed	700

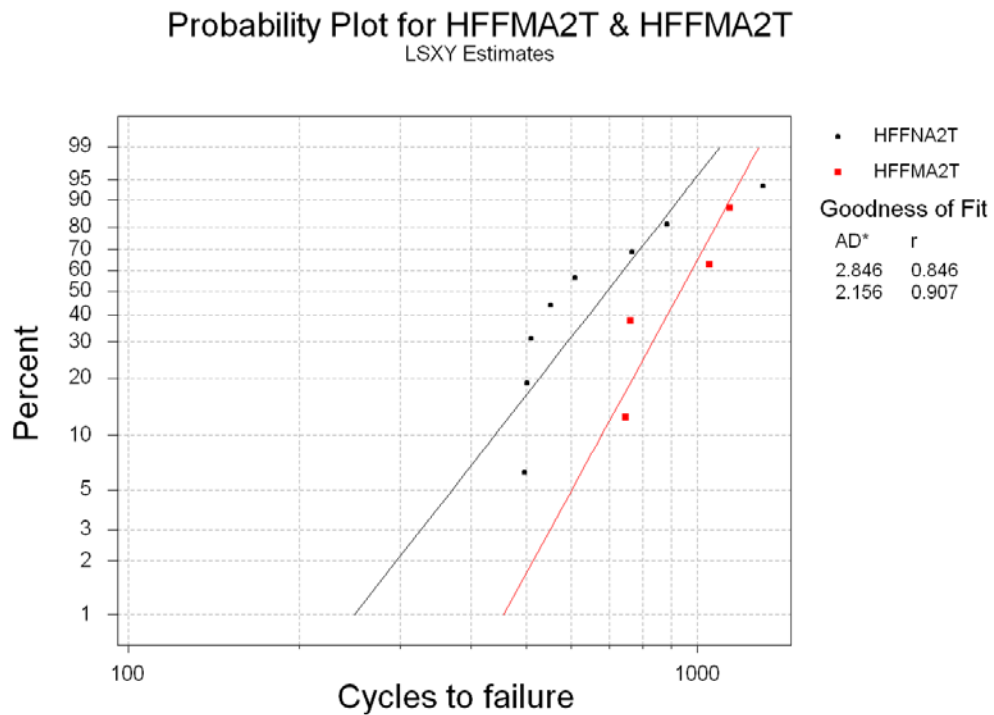


Figure 5: Weibull plot of thermal cycle failures for HFFNA2T (non-function pads included) and HFFMA2T (non-functional pads removed) for 2.5mm thick Ag finish PCBs, 10:1 vias.

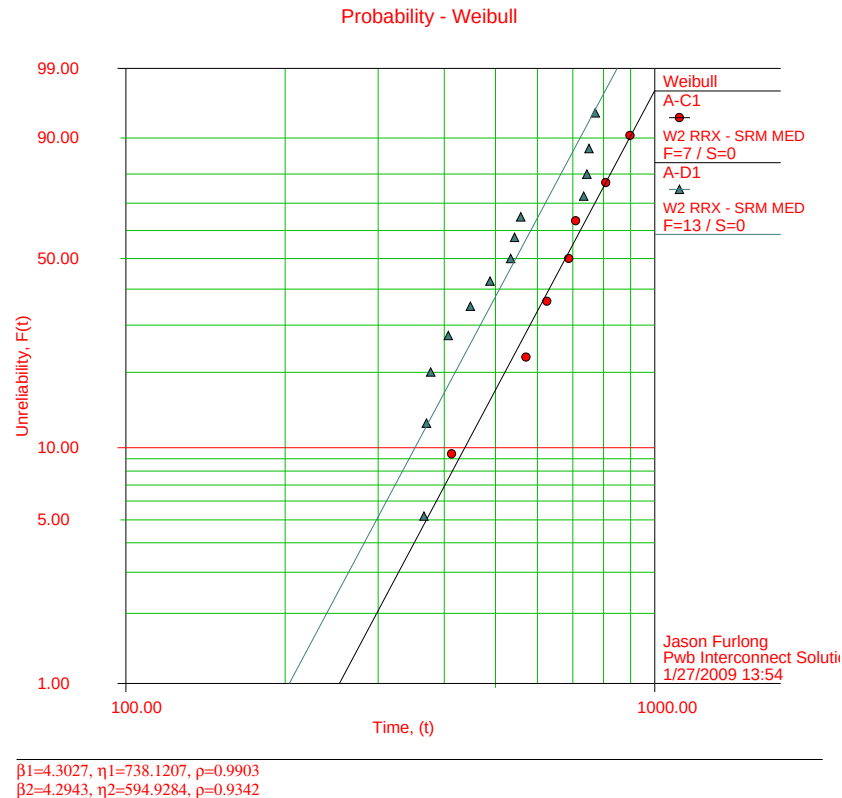


Figure 6: Weibull plot of IST failures for coupon D (non-function pads included) and coupon C (non-functional pads removed) for 2.5mm thick Ag finish PCBs, 10:1 vias.

3.2.1 Discussion of non-functional pads

Comparison of the results for the functional pads evaluation shows similar results for both thermal cycling and IST. For both techniques, the inclusion of non-functional pads caused early failures of the 10:1 aspect ratio vias, after conditioning for six lead-free reflow profiles, giving approximately a 20% reduction in fatigue life. A comparison for the number of cycles to 50% failures is given in Figure 7. This difference, although significant, should be considered second order alongside such issues as PCB manufacturing quality (copper plating quality & thickness) and materials characteristics (Tg, z-axis CTE).

Reviewing micro-sections of failed vias indicates a high percentage of vias with non-functional pads included, failed adjacent to the non-functional pads as shown in Figure 8, even though these are away from the central portion of the via, where failures would generally be expected to occur. This correlates well with other evaluations that have been undertaken by PWB (reference 4) and Kim et al (reference 1). It has been postulated that the inclusion of non-functional pads in high aspect ratio vias acted as stress concentrators, leading to the earlier failure.

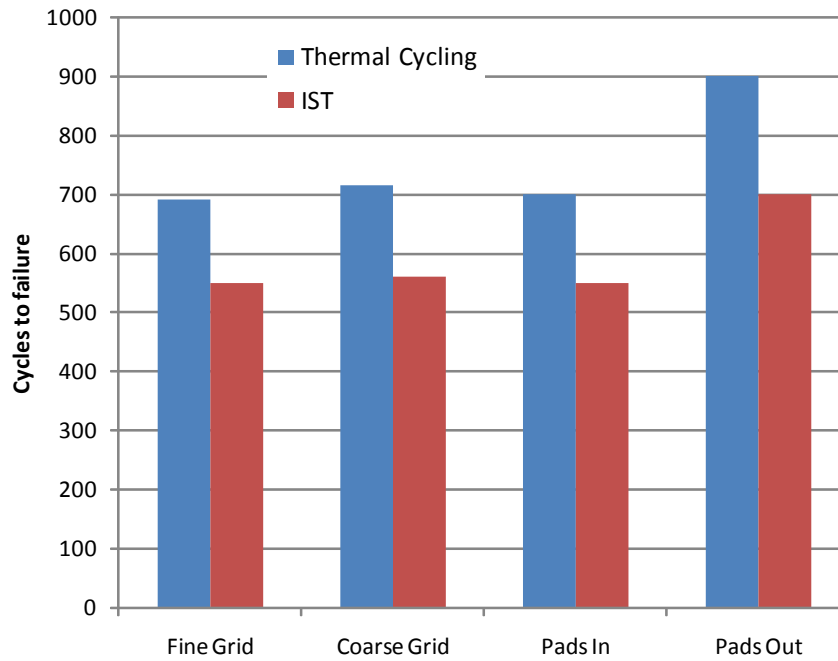


Figure 7: Comparison of number of cycles to 50% failures for thermal cycling and IST



Figure 8: Micro-section of via with failure in region where non-functional pads have been retained.

3.3 EFFECT OF GRID SIZE

As the each test substrate incorporated test structures for both the fine and coarse pitch grids, variances in the via wall thickness are not relevant and a direct comparison of results can be undertaken. The failures that were generated during thermal cycling for

samples with via grid pitches of 1.0mm and 0.8mm pitches, are shown in Figure 9, as a Weibull plot. The plot shows the similar gradients for both sample sets, with little difference between the relative reliabilities of both sample sets. The number of cycles to 50% failures is similar at around 700 thermal cycles (see Figure 7).

The failures that were generated during IST testing for samples with via grid pitches of 1.0mm and 0.8mm pitches, are shown in Figure 10 as a Weibull plot. The plot shows the similar gradients for both sample sets and little difference between the relative reliabilities of both sample sets. The number of cycles to 50% failures is similar at around 550 IST cycles.

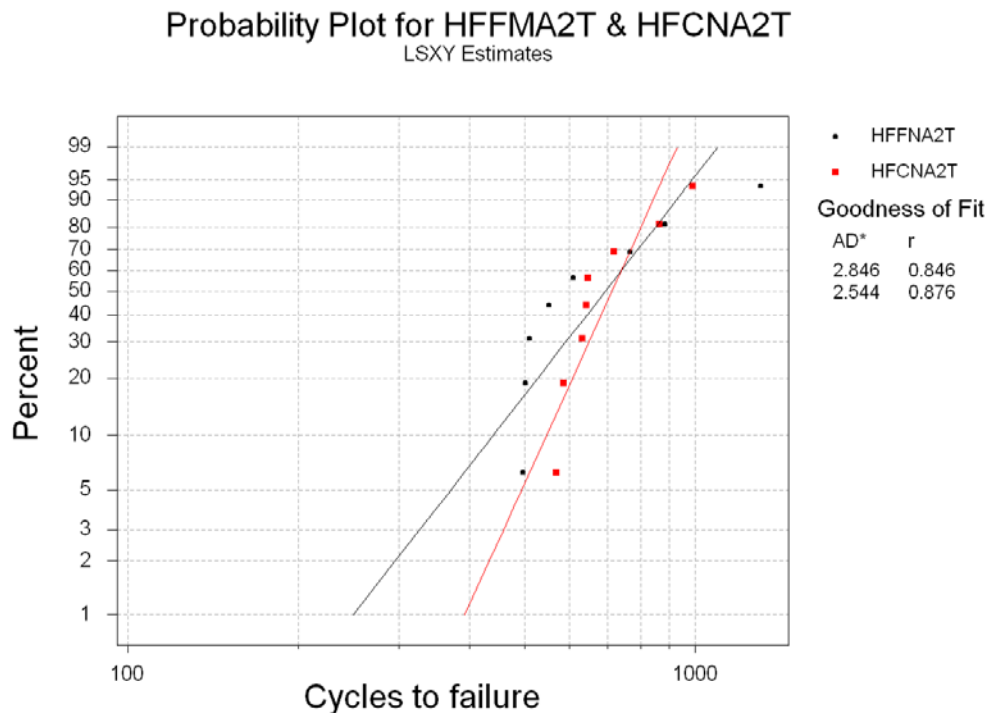


Figure 9: Weibull plot of thermal cycle failures for HFFNA2T (fine pitch grid) and HFCNA2T (coarse pitch grid) for 2.5mm thick Ag finish PCBs, 10:1 vias.

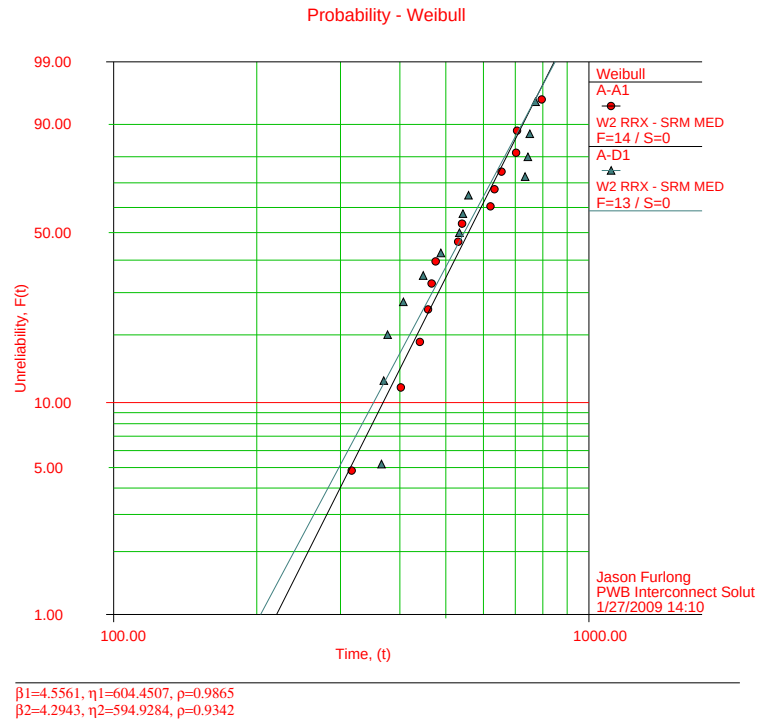


Figure 10: Weibull plot of IST failures for coupon D (fine pitch grid) and coupon A (coarse pitch) for 2.5mm thick Ag finish PCBs, 10:1 vias.

3.3.1 Discussion on grid size

The results comparing the effect of reducing the via grid size from 1.0mm to 0.8mm showed little effect for both thermal cycling and IST. The Weibull plot for the thermal cycle results (Figure 9) shows similar failure rates for both grid sizes. The number of cycles to 50% failures as shown in Figure 10 is also similar. Analysis of micro sections of failed vias from each data set also indicated similar failure modes and locations. Typical failures are shown in Figure 11 for a coarse pitch via and Figure 12 for a fine pitch via. The results for the IST are similar with no differentiation between the data sets.

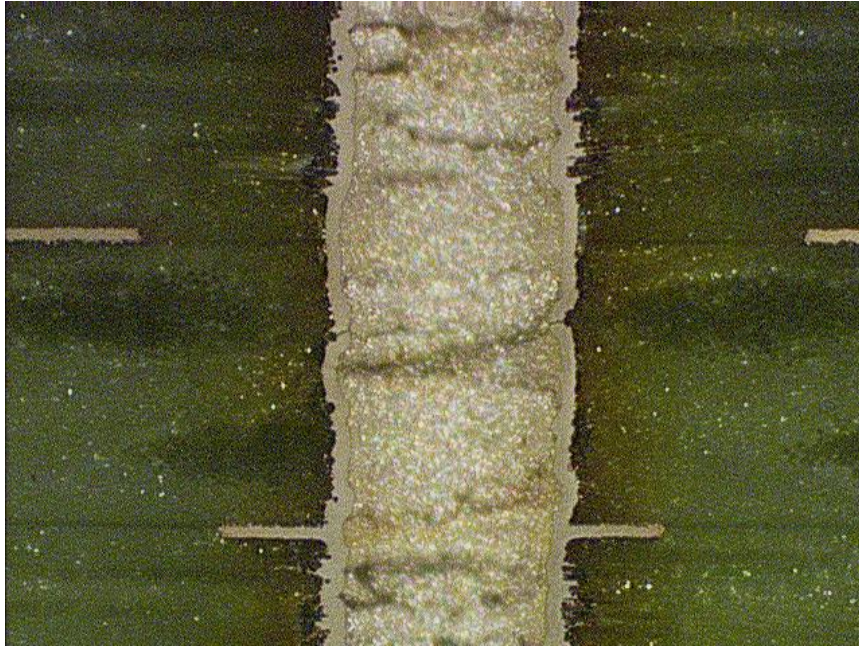


Figure 11: Micro-section of failure for via on coarse (1.0mm) pitch

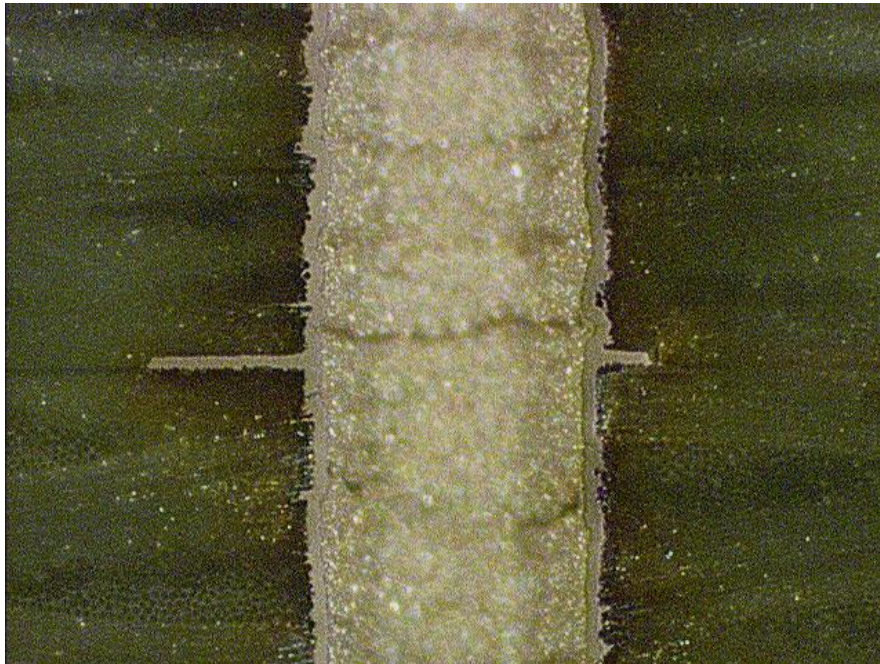


Figure 12: Micro-section of failure for via on fine (0.8mm) pitch

3.4 EFFECT OF PCB SURFACE FINISHES

The failure data for thermal cycling of the vias with different surface finishes are given in Figure 13 with the via wall thicknesses also noted. These thicknesses were similar for the ENIG, HASL and Ag finishes and although the minimum wall thicknesses are all below IPC minimum of 0.020mm, a direct comparison can be made.

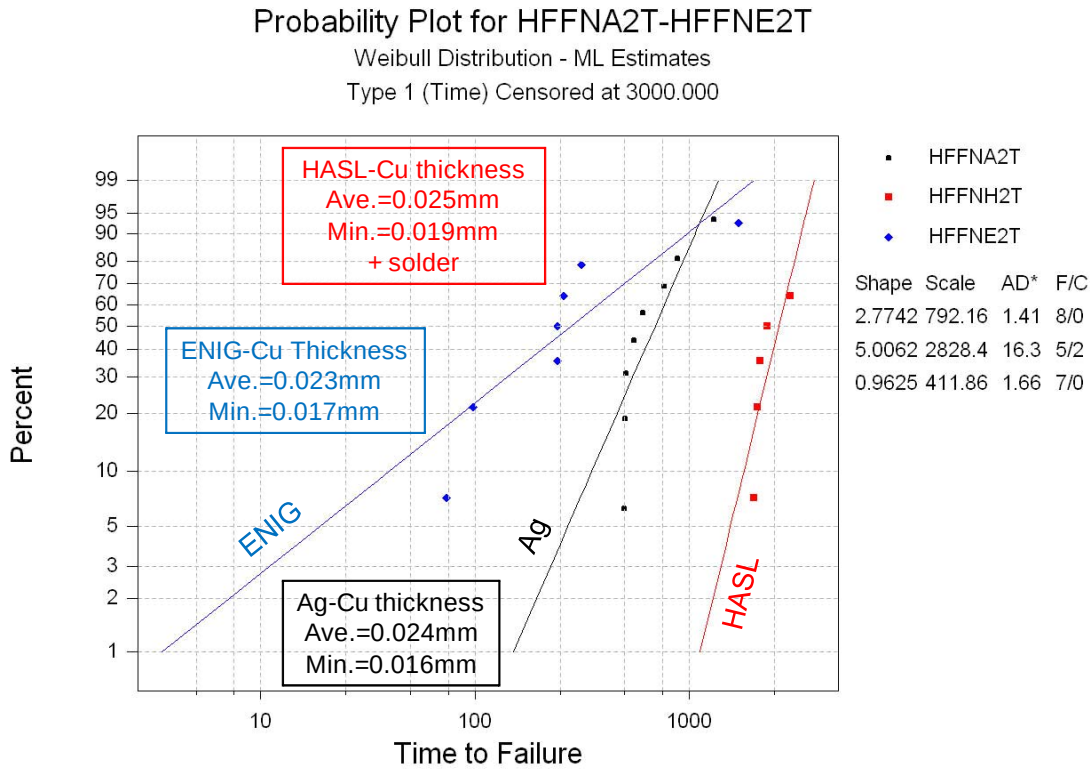


Figure 13: Comparison of thermal cycling results for PCB surface finishes for 10:1 vias, 6x260° C reflows, 2.5mm thickness, HP material, fine pitch grid

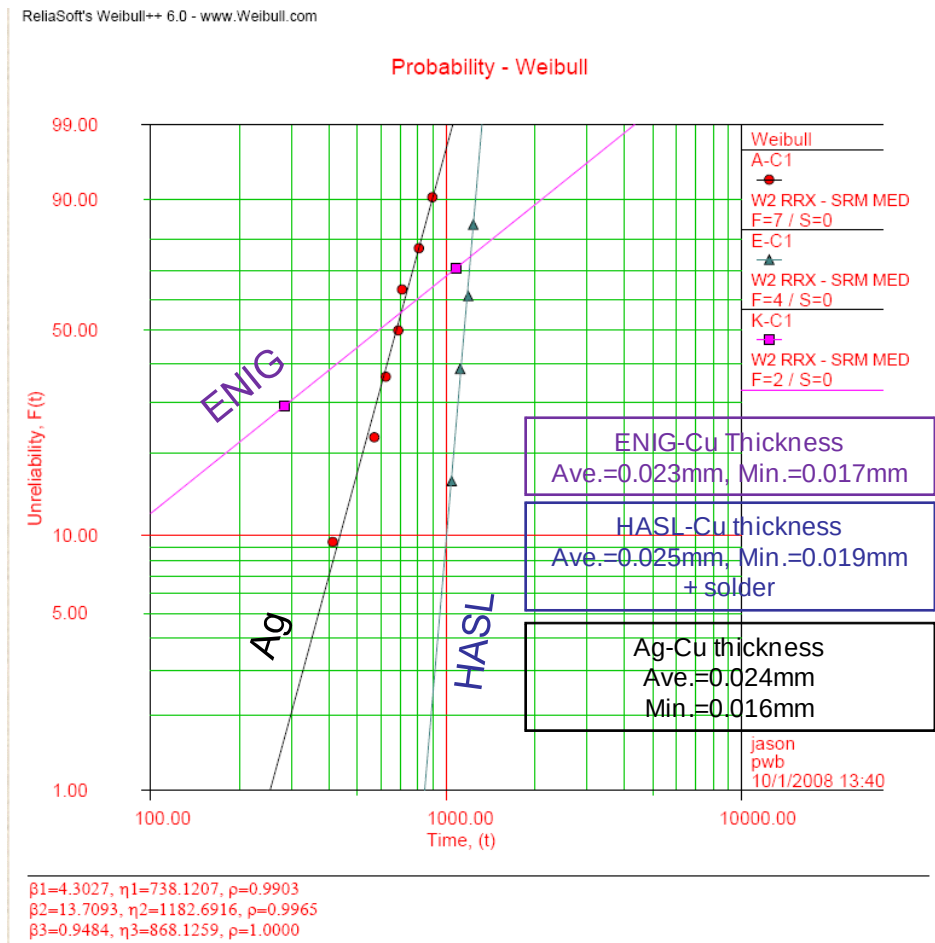


Figure 14: Comparison of IST results for PCB surface finishes for 10:1 vias, 6x260° C reflows, 2.5mm thickness, HP material, fine pitch grid

3.4.1 Discussion of PCB surface finish

Figure 13 and Figure 14 clearly show significant differences between the three surface finishes. The HASL finish vias outperformed the Ag finished vias and the reason for this can again be seen in micro-section, a typical example shown in Figure 15. The HASL process has deposited a solder coating down the walls of the via, strengthening the via. Measurements of the solder thickness showed an average of 0.030mm of solder with a minimum of 0.006mm. This results in better thermal cycling performance despite the fact that the HASL boards have been through an additional thermal stress during fabrication.

Normally, the ENIG surface finish would be expected to prove more reliable due to the presence of the nickel layer on the outer surface of the copper, which reinforces the wall of the via and can maintain via integrity even when the Cu has failed. However, micro-sections of ENIG finish vias indicate failure in the Ni layer first resulting in premature copper barrel failure. Figure 16 shows a typical ENIG barrel failure from outer wall inwards. Normal failure of an ENIG via would be in the opposite direction (reference 6)

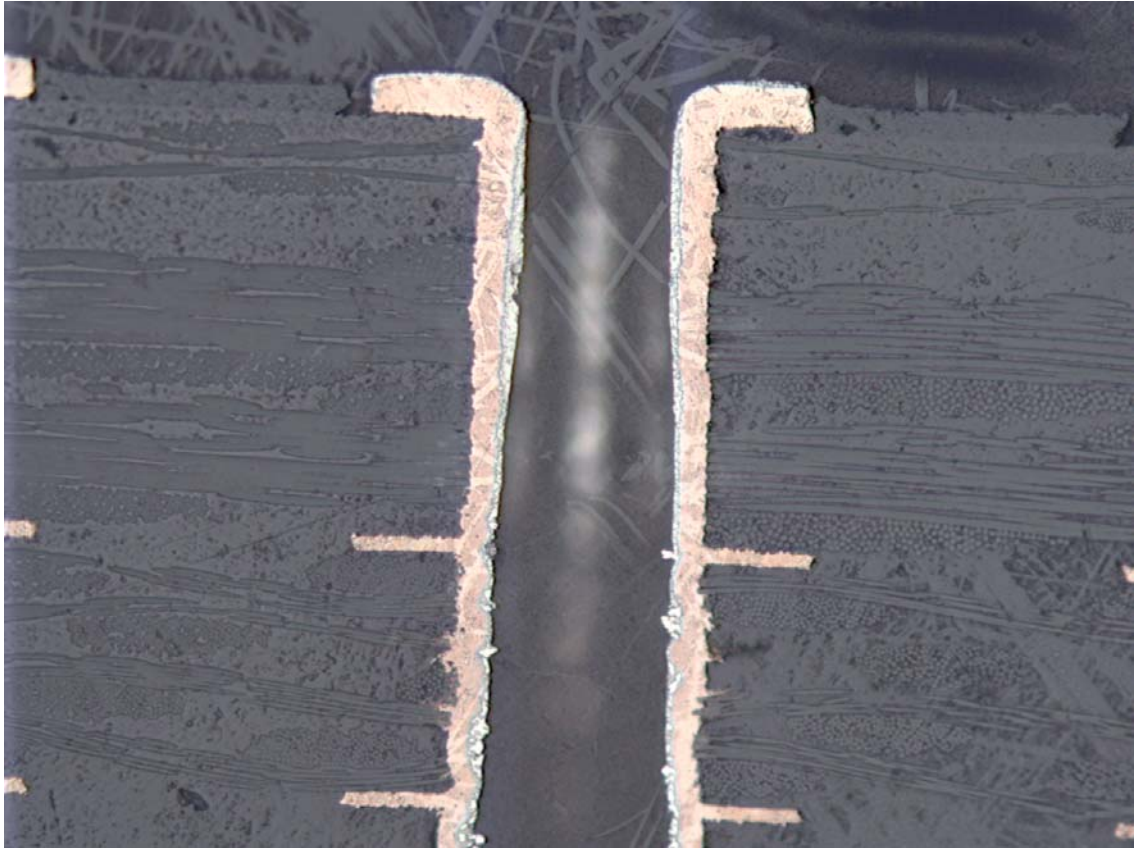


Figure 15: Microsection of HASL via showing solder coating of the via

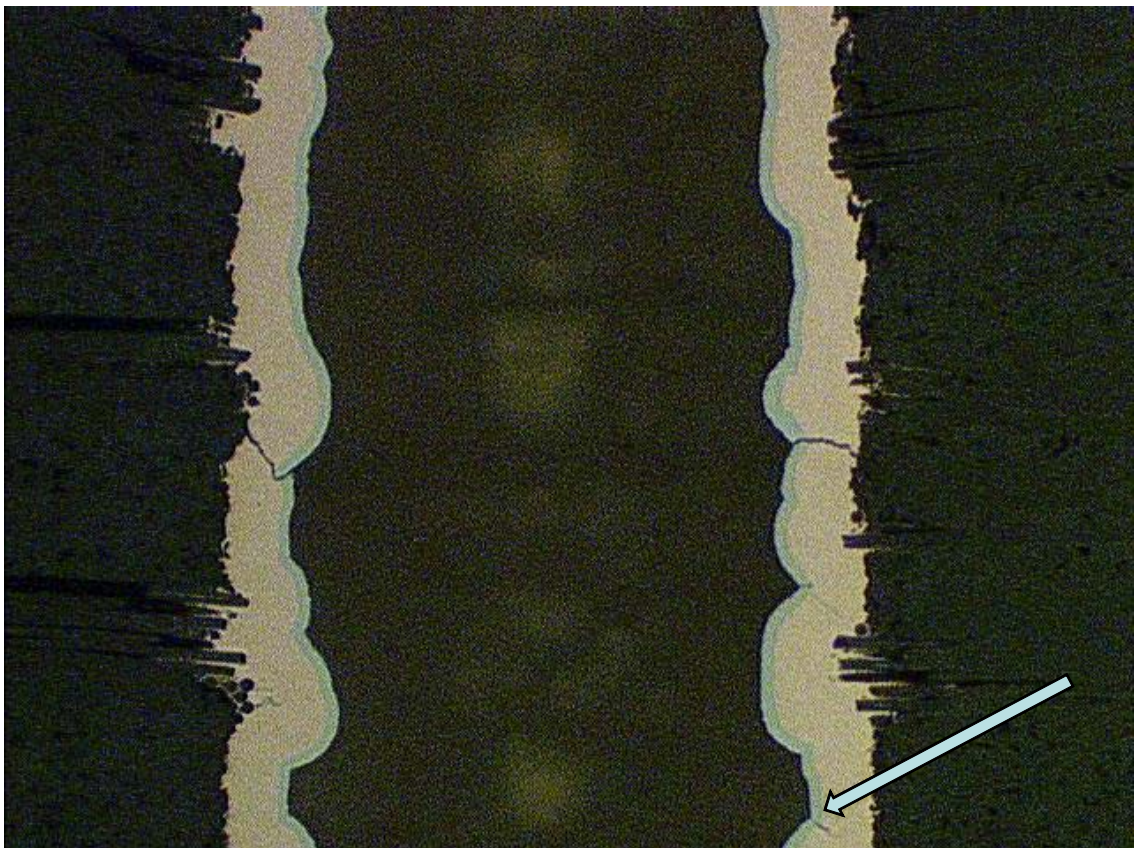


Figure 16: Typical failure in ENIG PCB showing early failure of nickel layer

3.5 EFFECT OF PCB THICKNESSES

The thermal cycling failure data for the vias of different PCB thicknesses are given in Figure 17, with the via wall thicknesses also noted. These thicknesses were similar for the 1.6mm and 2.5mm thick PCB, but the wall thickness for the 3.2mm thick PCBs was significantly less. It should be noted that the wall thicknesses were all below IPC class 3 minimum of 0.020mm.

There were no IST failures for the 1.6mm thick test vehicles. The 3.2mm thick samples were un-testable as via degradation was too advanced after 6 reflows to allow stable measurement of via conductivity. The results for the 2.5mm thick PCBs are given in Figure 18.

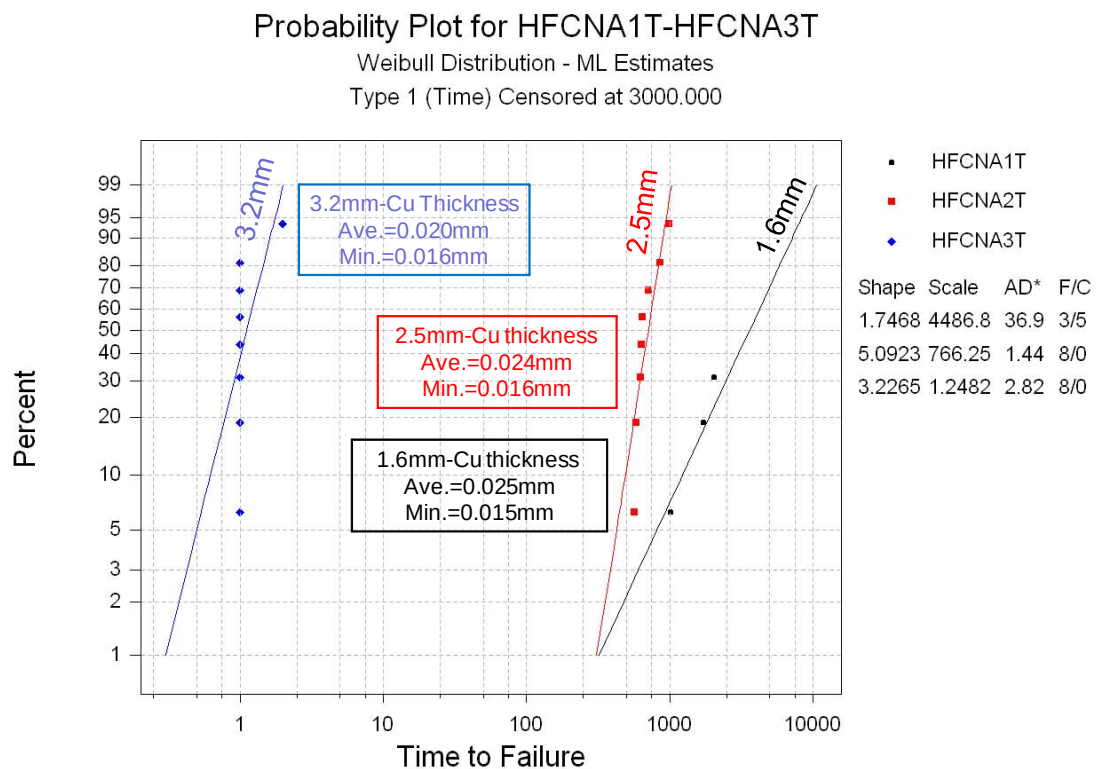


Figure 17: Comparison of thermal cycling results for PCB thickness for 10:1 vias, 6x260° reflows, Ag finish, HP material, coarse pitch grid

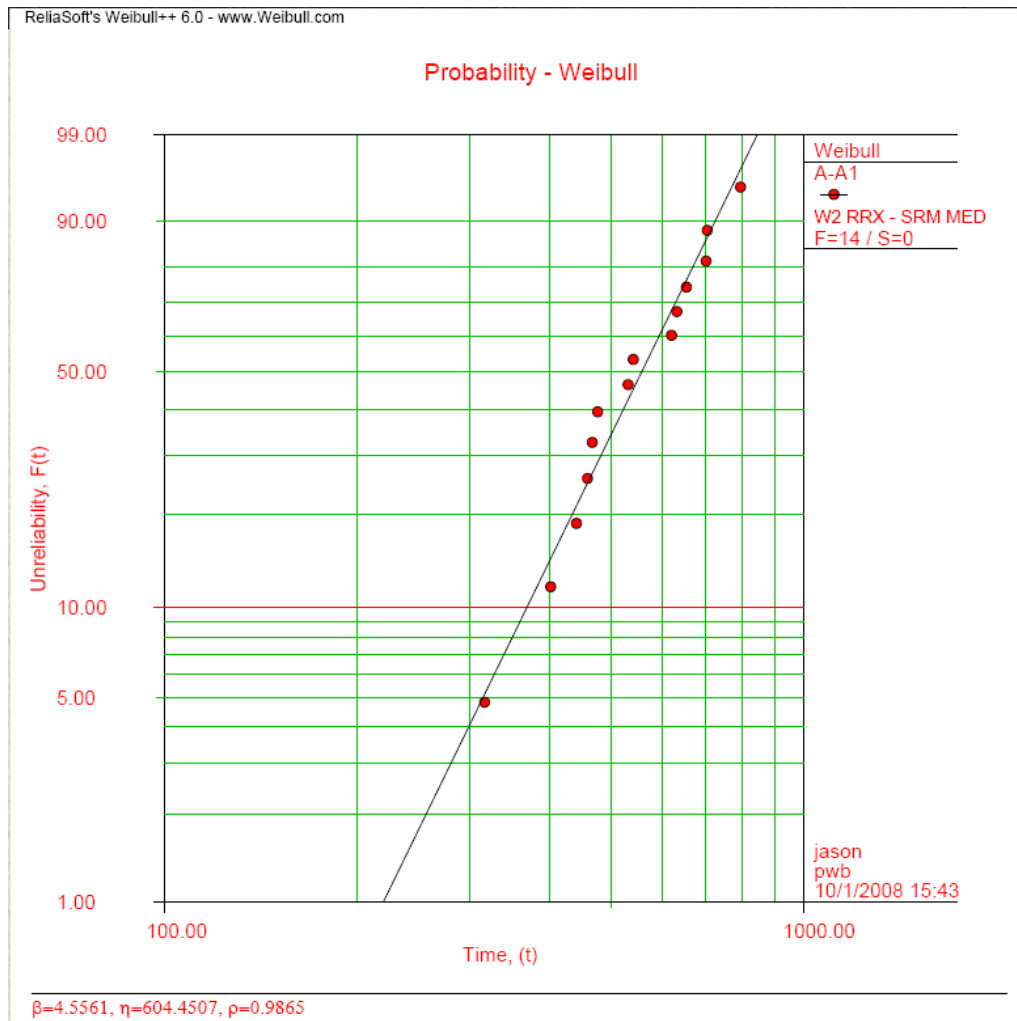


Figure 18: Comparison of IST results for 2.5mm PCB thickness for 10:1 vias, 6x260° reflows, Ag finish, HP material, coarse pitch grid

3.5.1 Discussion of PCB thickness

The average via wall thickness was less for 3.2mm boards than for 2.5 or 1.6mm thick PCBs and therefore direct comparison of all three is not possible. Figure 19 shows the expansion that would be expected for different PCB thicknesses as the PCB is heated from room temperature to 260°C in a reflow soldering operation. Thicker PCBs would be expected to expand more, placing greater stress on the via wall and causing more degradation caused during profiling. Coupled with weakening of the via due to thinner copper, this is the cause of the early failure of the 3.2mm thick PCBs. Direct comparison of the 2.5 and 1.6mm thick PCBs is possible, as via wall thicknesses are comparable and here the thicker PCB can be seen to have a lower reliability, consistent with the increased stress placed on the vias during conditioning (see Figure 17).

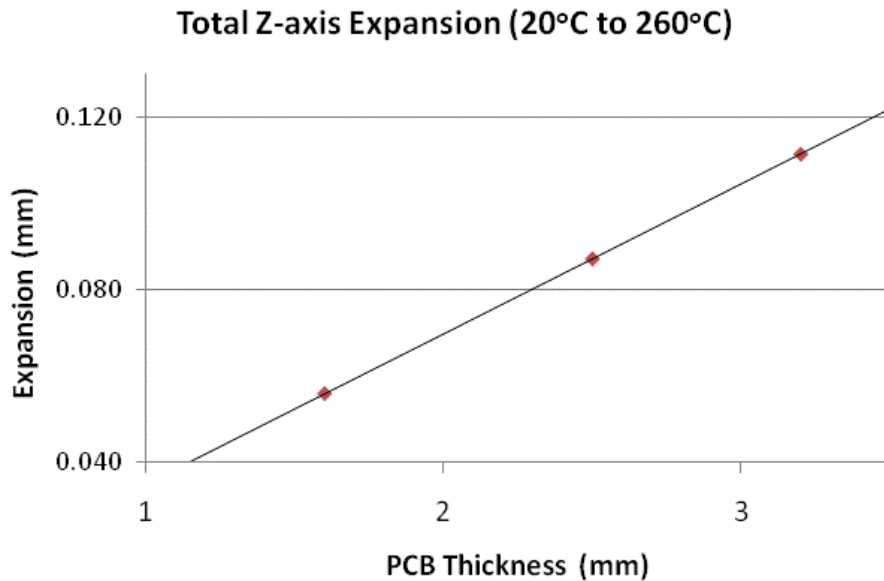


Figure 19: Calculated z-axis expansion for different PCB thicknesses during reflow soldering

3.6 EFFECT OF CONDITIONING PCBS

The failure data for thermal cycling of the vias for different degrees of conditioning are given in Figure 20, with the via wall thicknesses also noted. Failure data for IST are given in Figure 21. These thicknesses for all four sets of test PCBs were different and therefore direct comparison of results is not possible.

3.6.1 Discussion of conditioning PCBs

The results for the PCBs subjected to 6 reflows were significantly worse than for the other types of conditioning and this was probably due to the much thinner via wall thicknesses of these samples. This also explains why the addition of 2 rework profiles appears to improve reliability, when it might be expected to have no effect or to reduce reliability. The wall thickness for this latter group was approximately 30% greater. However, it should be noted that the reliability of the samples subjected to two wave soldering profiles was better than for the 6R+2RW PCBs even though their wall thickness was less on average. Thus the conditioning of two wave soldering profiles can be considered to be more benign than 6R+2RW. There was little difference in via wall thickness or reliability for 6R+2RW or 3R+2RW conditioning.

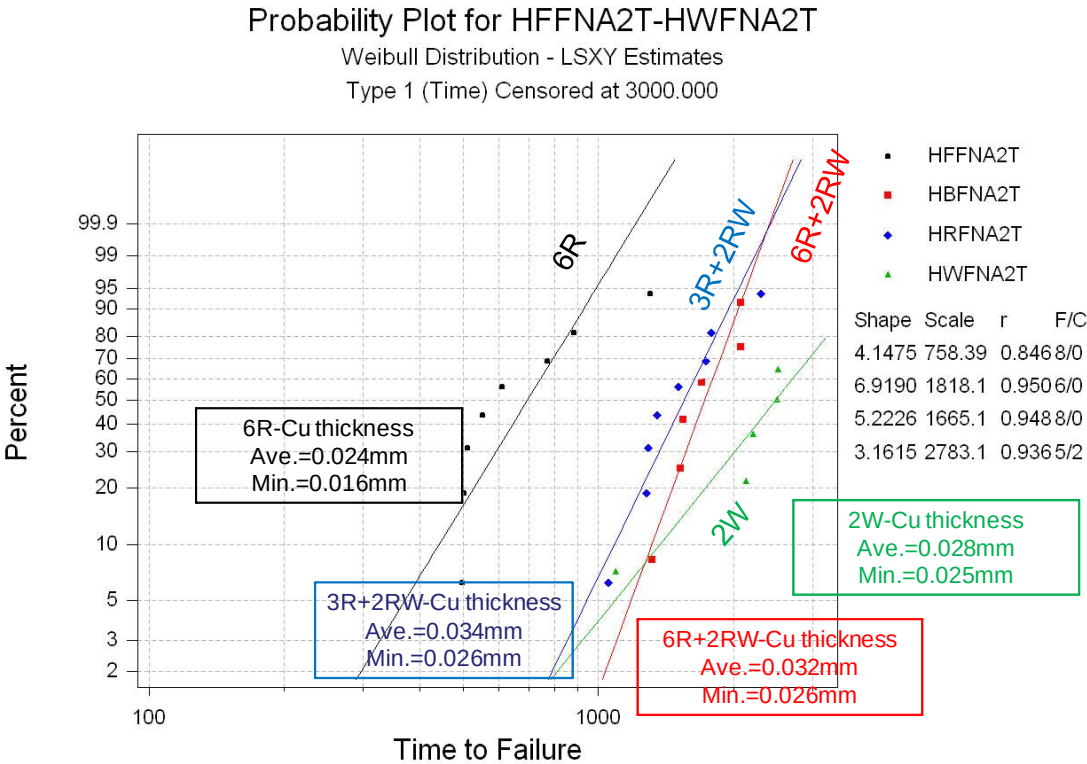


Figure 20: Comparison of thermal cycling results for conditioning of 10:1 vias, Ag finish, 2.5mm thickness, HP material, fine pitch grid

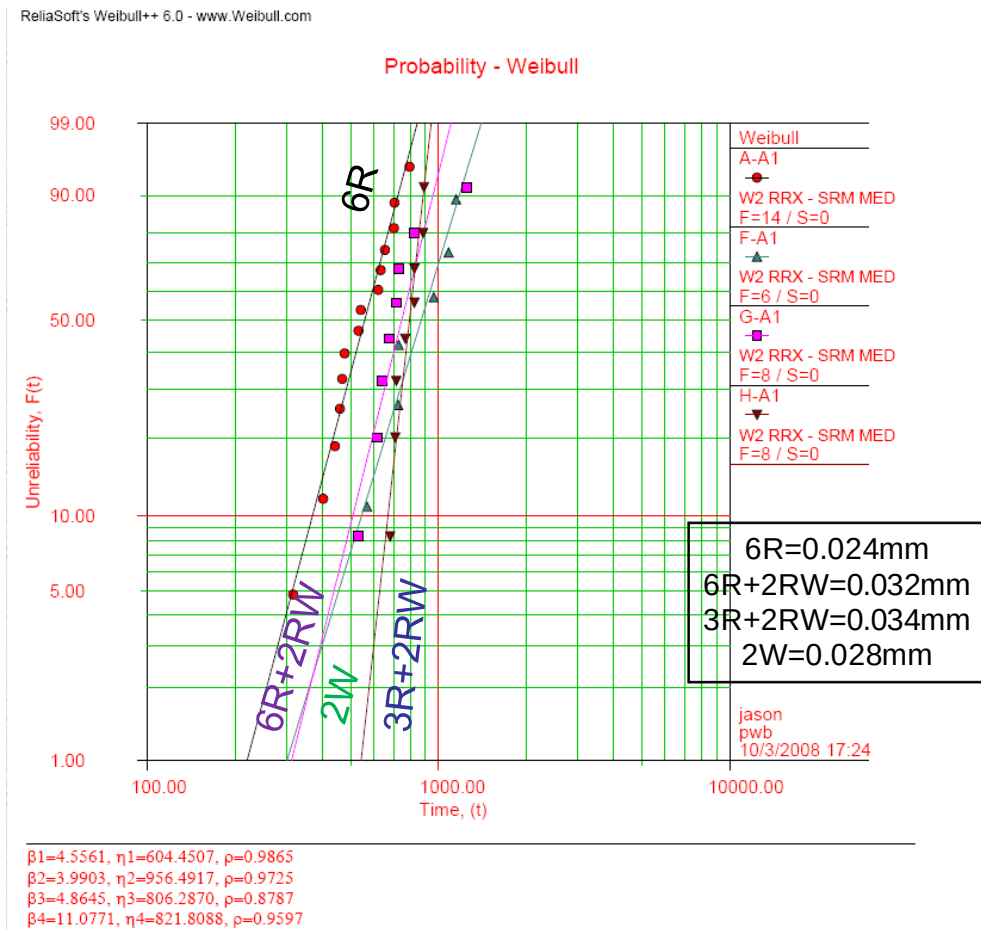


Figure 21: Comparison of IST results for PCB conditioning for 10:1 vias, Ag finish, 2.5mm thickness, HP material, fine pitch grid

3.7 EFFECT OF DIFFERENT PCB MATERIALS

The failure data for thermal cycling of the vias for different PCB materials are given in Figure 22 with the via wall thicknesses also noted. These thicknesses for both sets of data are similar and therefore a direct comparison of results is possible. IST testing of the polyimide PCBs did not produce any via failures. IST results for the HP material are shown in Figure 18.

3.7.1 Discussion on PCB materials

Both the thermal cycling and IST results indicate the polyimide material has an increased reliability over the HP. Calculated values for N(1%) failures due to thermal cycling are shown in Figure 24. The polyimide has a higher T_g than the HP material (see 3.17), with this T_g being above the peak reflow temperature. Thus, during the conditioning reflows, the vias in the HP material are under greater stress due to the increased expansion of this material above the T_g of the HP materials (270 compared to 70 ppm/°C, see 3.18)

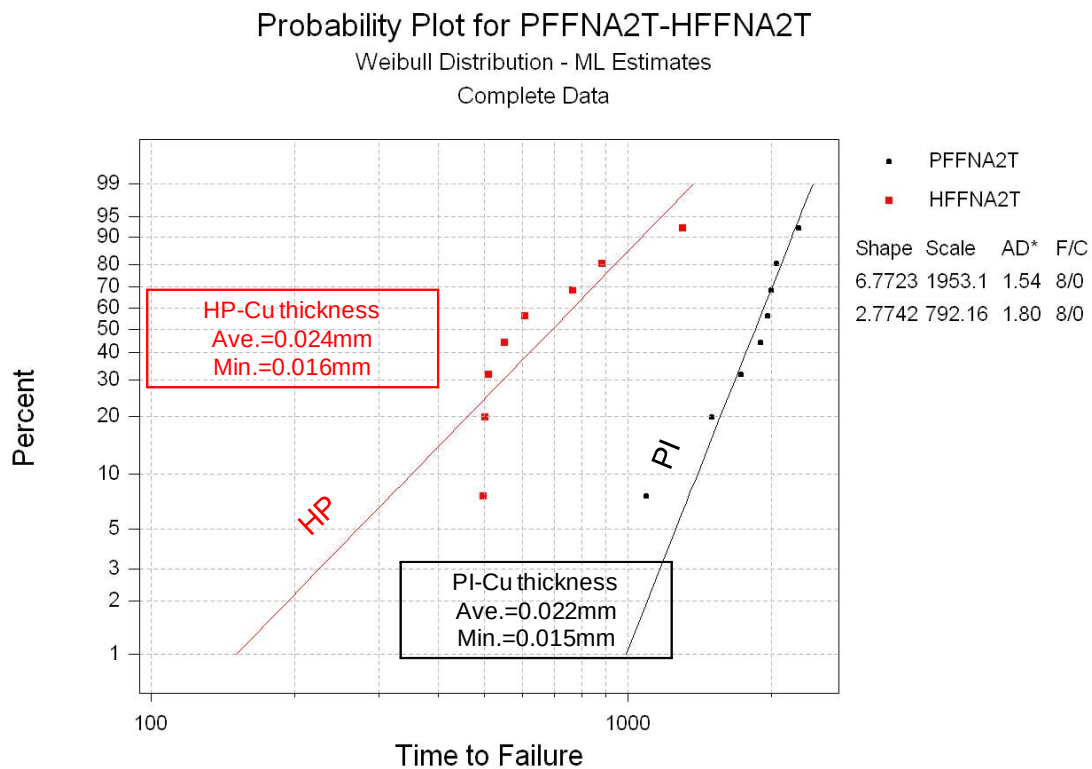


Figure 22: Comparison of thermal cycling results for PI and HP materials for 10:1 vias, Ag finish, 2.5mm thickness, fine pitch grid

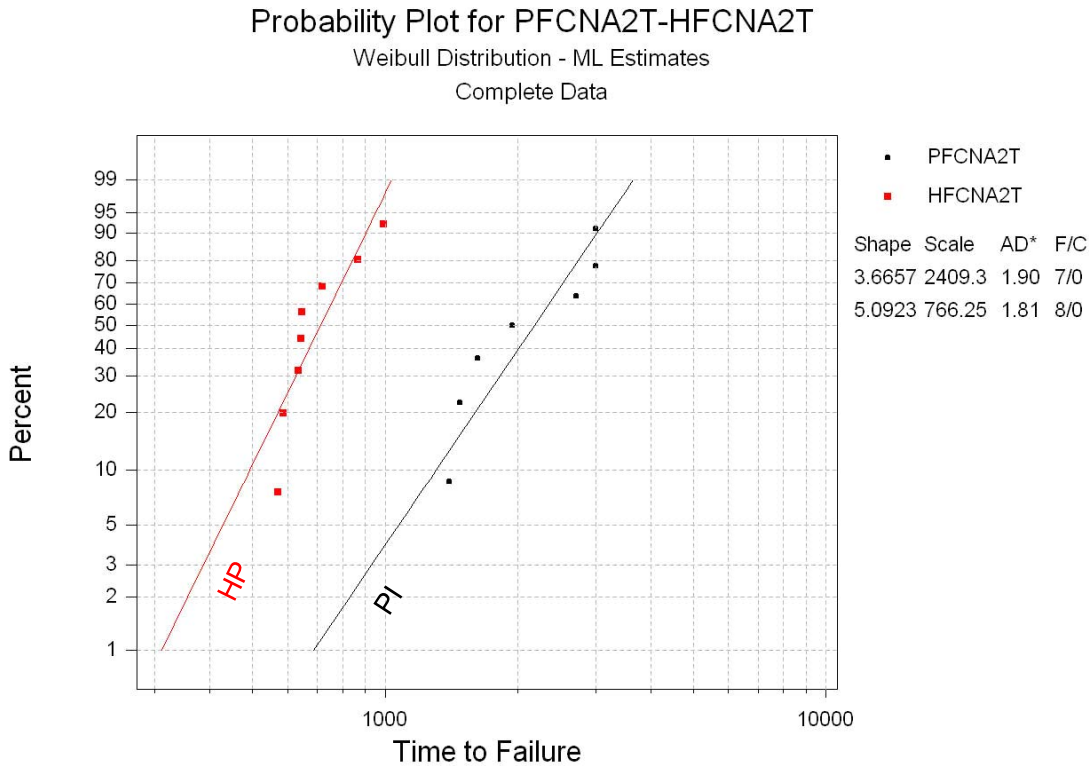


Figure 23: Comparison of thermal cycling results for PI and HP materials for 10:1 vias, Ag finish, 2.5mm thickness, coarse pitch grid

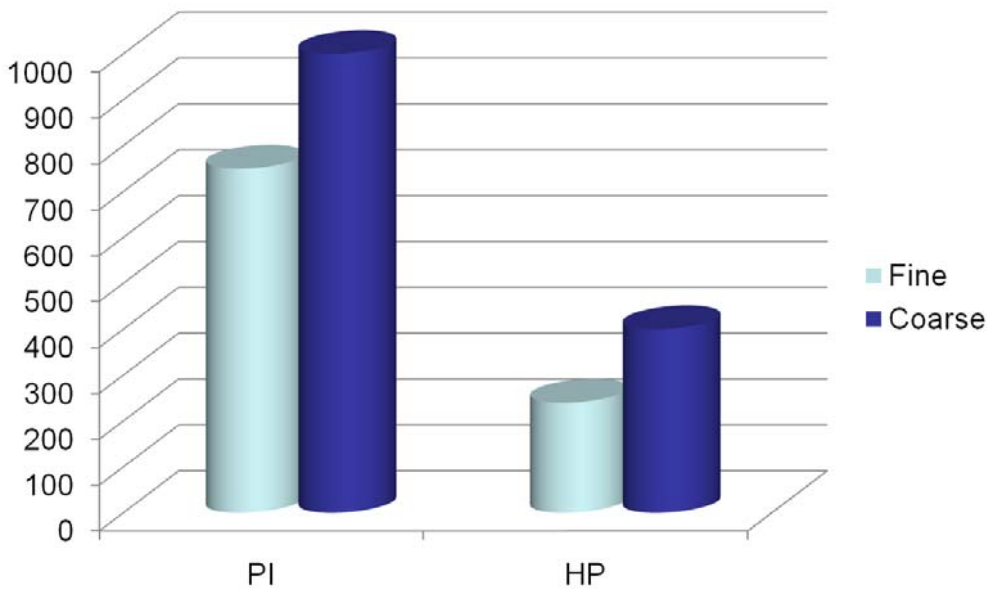


Figure 24: N(1%) failure comparison for thermal cycling

3.8 EFFECT OF THERMAL CYCLING OF MICROVIAS

Failures in the μ vias chains are given in Table 4.

Table 4: Thermal cycling μ Via failures

Board Nos	Material	Surface Finish	Thickness	Conditioning	No of failures at 3000 cycles	Failure range (cycles)
11-14	HP	Ag	2.5mm	6R	6	1051 to 2344
31-34	HP	Ag	3.2mm	6R	3	1785 to 1832
41-44	HP	Ag	1.6mm	6R	5	2141 to 2244
51-54	HP	LF HASL	2.5mm	6R	2	2074, 2088
61-64	HP	Ag	2.5mm	2W	0	
71-74	HP	Ag	2.5mm	6R + 2 BGA	0	
81-84	HP	Ag	2.5mm	3R + 2 BGA	3	1500 to 2075
91-94	PI	Ag	2.5mm	6R	2	1462, 2012
101-114	PI	ENIG	2.5mm	6R	1	121
111-114	HP	ENIG	2.5mm	6R	3	239 to 726

3.8.1 Discussion of thermal cycling of microvias

Generally there were insufficient failures at 3000 thermal cycles to compare reliability, although clearly the μ vias proved more reliable than through vias.

3.9 RESULTS OF DMA MEASUREMENTS OF TG

Figures 27 to 29 show the DMA results for as-received and conditioned HP material, and conditioned PI material. From this data, the Tg values in Table 5 can be calculated. The expansion of the unconstrained z-axis of the PCBs varies considerably above and below the Tg (see 3.18). Thus the higher Tg of the polyimide substrates would result in less thermal expansion during soldering as it's glass transition temperature would only be reached at the very hottest part of the soldering cycle, resulting in a lower stress being placed on the vias during soldering. Conditioning of the HP material did not change it's glass transition temperature.

Table 5: Calculated Tg values

Material	Glass Transition Temperature (Tg)
As-received high Tg phenolic cured epoxy	171°C
Conditioned (6 reflows) high Tg phenolic cured epoxy	170°C
Conditioned (6 reflows) polyimide	260°C

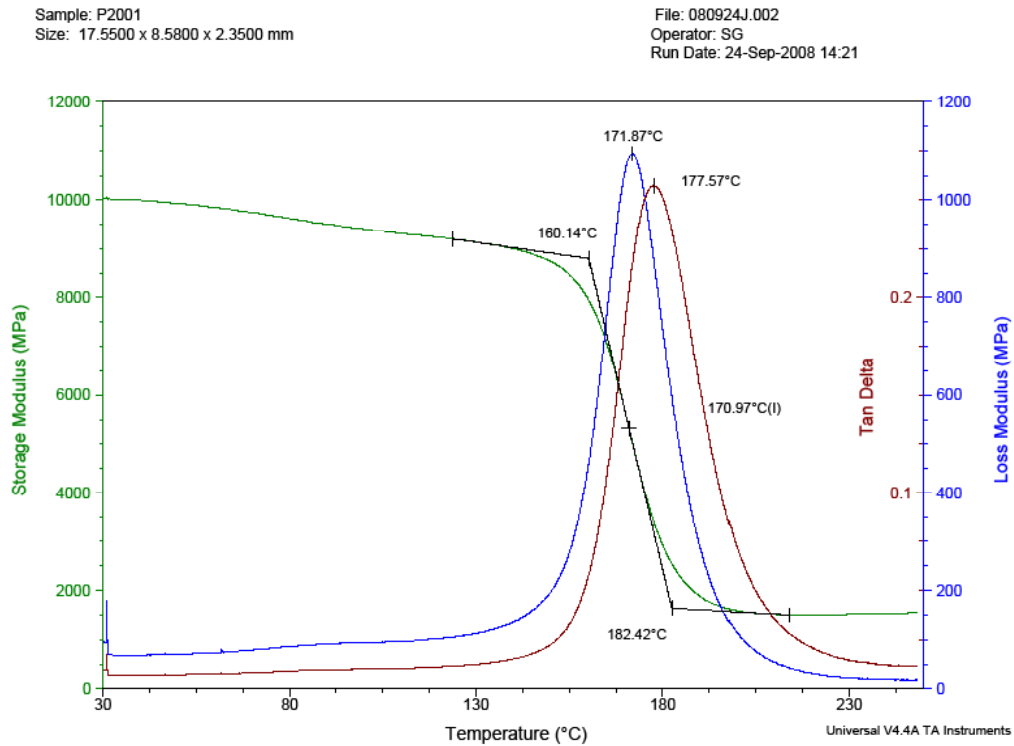


Figure 25: DMA measurements on as-received high Tg phenolic cured epoxy (HP) PCB, 2.5mm thickness

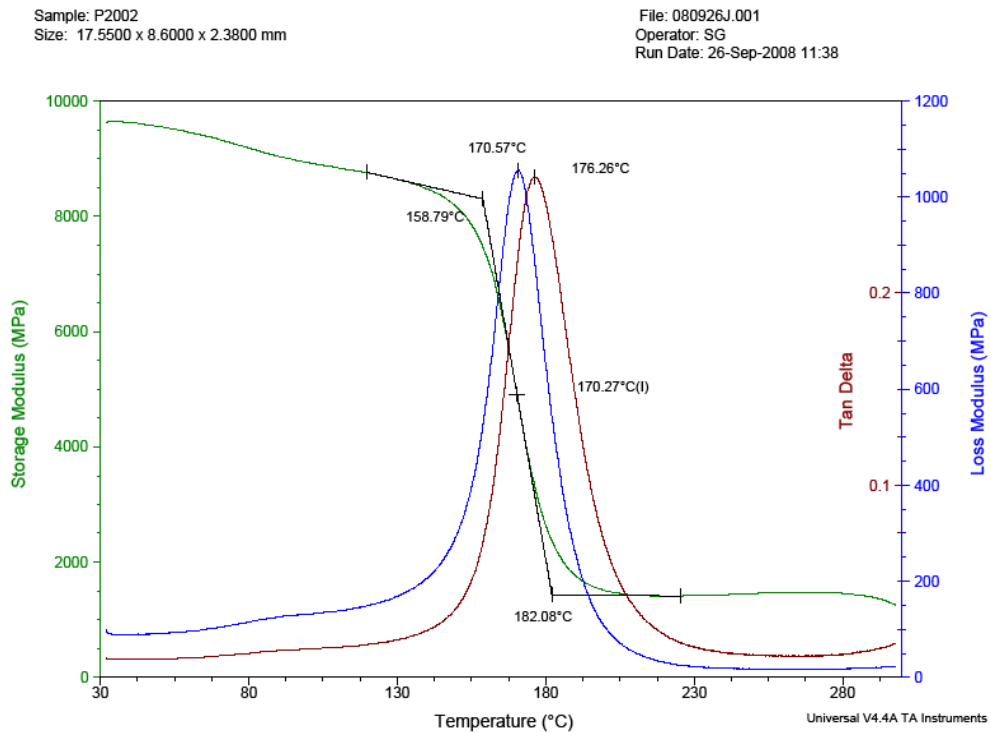


Figure 26: DMA measurements on conditioned (6 reflows) high Tg phenolic cured epoxy (HP) PCB, 2.5mm thickness

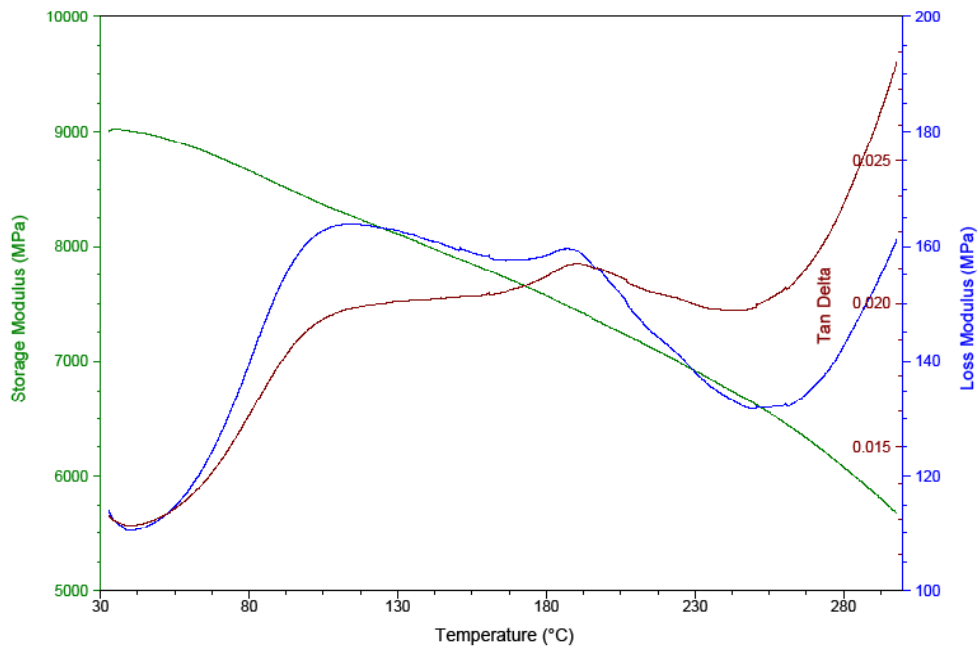


Figure 27: DMA measurements on conditioned (6 reflows) polyimide (PI) PCB, 2.5mm thickness

3.10 RESULTS FOR TMA MEASUREMENTS

Figure 28 and Figure 29 show the TMA results for the HP and PI material. From this data, the CTE values in Table 6 can be calculated. For both materials, below their Tg's, z-axis expansion is similar. However about Tg, the HP material has a significantly higher expansion coefficient.

Table 6: Calculated Z-axis CTE values

Material	CTE below Tg	CTE above Tg
High Tg phenolic cured epoxy (HP)	70ppm/°C	270ppm/°C
Polyimide (PI)	73ppm/°C	N/A

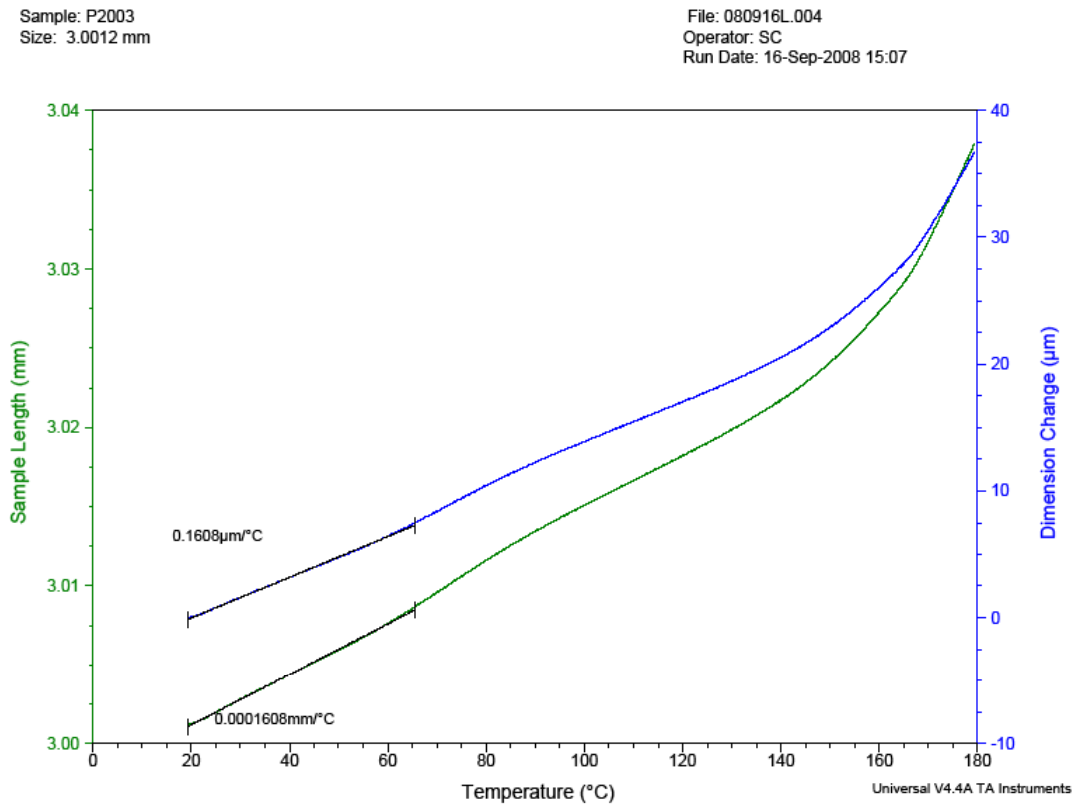


Figure 28: TMA measurements on conditioned (6 reflows) high Tg phenolic cured epoxy (HP) PCB, 3.2mm thickness

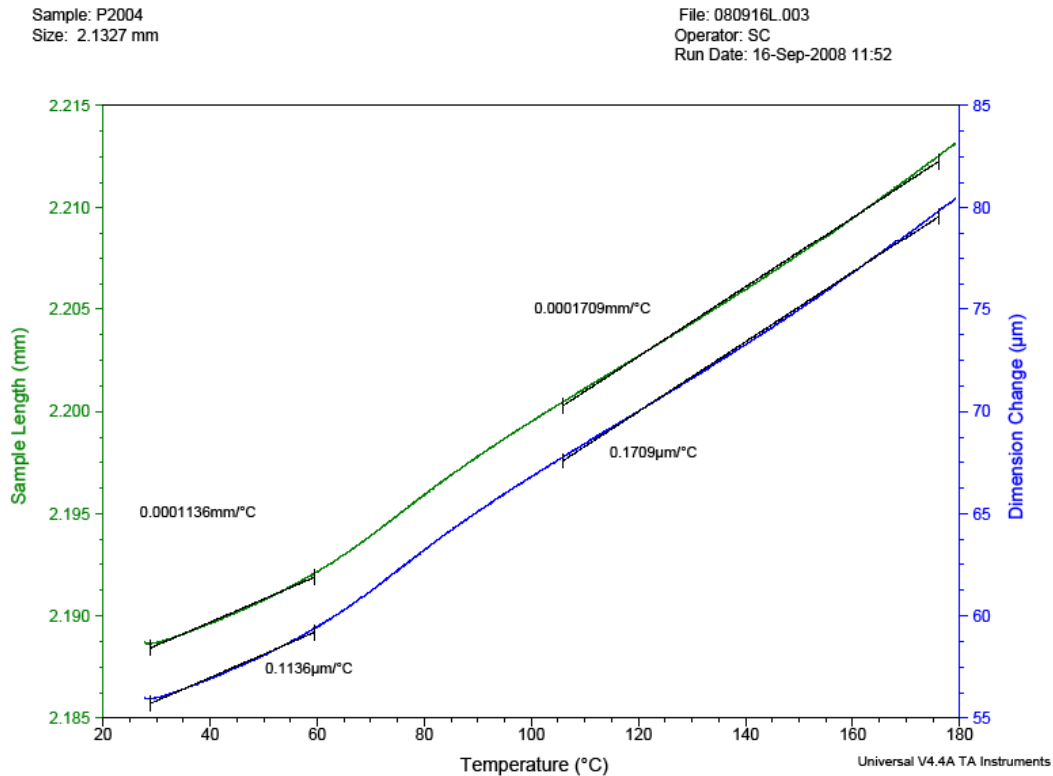


Figure 29: TMA measurements on conditioned (6 reflows) polyimide (PI) PCB, 2.5mm thickness

3.11 COMPARISON OF THERMAL CYCLING AND IST DATA

The results generated by both thermal cycling and IST for comparable via wall thicknesses, showed extremely good correlation. A comparison for the number of cycles to 50% failures is given in Figure 7 for the both sets of results. In all cases, failures occurred slightly earlier for IST than for thermal cycling. This is explained by the 25°C higher test temperature and the more stringent failure criteria for the IST test method. For thermal cycling, a via chain is considered to have failed when the resistance increases to greater than 5k Ω for a period greater than 200ns. For IST, measuring a 10% increase in resistance of the via chain is considered a failure. Allowing for these differences, both techniques gave similar results with 50% failures occurring in the 500 to 900 cycles range. The relative ranking of the level of failures is identical for both the thermal cycling and IST. It should be noted that these results were obtained in very different timescales. For the thermal cycling, 1000 cycles takes about 40 days of testing although multiple circuits can be tested simultaneously. The test setup used here was capable of monitoring 480 circuits continuously during those 40 days. IST testing was undertaken in a much shorter time frame with 1000 cycles taking approximately 4 days to complete. However, during this period, each IST tester can only monitor 12 test circuits. Therefore, IST gives fast comparable results, but thermal cycling may be more beneficial if a wide range of experimental parameters were to be tested simultaneously.

4 CONCLUSIONS

The National Physical Laboratory and PWB Interconnect Solutions Inc. have successfully completed a joint reliability study on identical test structures using thermal cycling with constant electrical monitoring (event detecting) and IST. The coupons included test patterns to monitor changes in interconnection pitch and also the effect of the removal of non-functional pads. The failure modes generated with both techniques were similar as were the relative rankings of the effects. The results showed that the removal of non-functional pads improved reliability by 20% for high aspect ratio plated through holes in thicker substrates. However this effect should be considered second order alongside such issues as PCB manufacturing quality (copper plating quality or thickness) and materials characteristics (T_g , z-axis CTE). Decreasing interconnection pitch from 1.0mm to 0.8mm had little effect on failure rate.

The results for the PCBs with different surface finishes showed that ENIG performed significantly worse than expected. This was due to poor nickel quality down the vias, leading to rupture of the nickel and subsequent premature failure of the under laying copper barrel. The PCBs with HASL finish performed better than those with Ag finish, due to presence of solder down the vias.

During testing the PCBs of the greatest thickness (3.2mm) failed very early. Micro-sectioning showed they had thin copper (average 0.02mm) and this, coupled to their greater thickness and hence greater z-axis expansion during soldering, caused this earlier demise. The 1.6mm thick PCBs performed better than the thicker boards as these substrates generated lower stresses on vias during reflow as their z-axis expansion was less.

Subjecting the PCBs to different reflow and rework conditioning was difficult to interpret due to varying copper barrel plating thicknesses between sample sets. Those substrates subjected to six reflow operations performed worst but also had significantly thinner copper barrel plating. No significant differences could be determined between 6 reflows + 2 BGA reworks, 3 reflows + 2 BGA reworks and 2 wave soldering operations, although the copper barrel plating thickness on wave soldered samples was thinner than the other two conditions, implying that this conditioning was more benign.

Polyimide substrates consistently out-performed the high T_g phenolic cured epoxy PCBs. The polyimide has higher T_g than the peak temperature for the reflow conditioning and thus during conditioning, the HP material exhibited a higher z-axis CTE (270 compared to 70 ppm/ $^{\circ}$ C), causing greater stress on the vias.

For the μ vias test patterns, there were insufficient failures during testing to compare reliability between the different experimental variables. However, there is sufficient data to determine that the μ vias were more reliable than the through vias.

The results generated by both thermal cycling and IST showed extremely good correlation. Failures occurred slightly earlier for IST than for thermal cycling. This is explained by the 25 $^{\circ}$ C higher test temperature and the more stringent failure criteria applied for IST test method. Allowing for these differences, both techniques gave similar results with 50% failures occurring in the 500 to 900 cycles range. The relative ranking of the level of failures is identical for both the thermal cycling and IST but the

results were obtained in very different timescales. In this specific study results were achieved in 2 to 3 days with IST versus 20 to 40 days with the thermal oven. IST has been shown to give fast comparable results to thermal cycle testing with constant monitoring, but thermal cycling may be more beneficial if a wide range of experimental parameters is to be tested simultaneously.

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