

Report

NPL REPORT MAT 10

Reliability of Electronic Substrates After Processing at Lead-free Soldering Temperatures

**M Wickham, M Dusek and
C Hunt**

NOT RESTRICTED

DECEMBER 2007

Reliability of Electronic Substrates After Processing at Lead-free Soldering Temperatures

Martin Wickham, Milos Dusek and Christopher Hunt
Industry and Innovation Division

ABSTRACT

The requirement to comply with European RoHS regulations which ban the use of lead, is driving the adoption of new materials both in PCB assembly and bare board manufacture. The alloy traditionally used for soldering in electronics manufacture, SnPb, can no longer be used. But the preferred replacement (a tin/silver/copper alloy) has a higher melting point of $\sim 217^{\circ}\text{C}$, and concern has been expressed that the higher stresses involved during lead-free processing may affect the reliability of the PC substrates. In consequence this collaborative study aimed to

- (i) provide the electronics manufacturing industry with a test method for measuring the effect of the higher temperatures associated with lead-free soldering on the reliability of electronic substrates
- (ii) improve industry confidence in the reliability of PCB substrates during and after the change to lead-free processes.

This study investigated the reliability of daisy-chained vias in four commonly used types of laminate materials - both standard and high glass transition temperature (T_g) epoxy systems, with both dicy and phenolic curing agents. The assemblies were conditioned prior to thermal cycling using reflow soldering profiles with peak soldering temperatures of 230, 245 or 260 $^{\circ}\text{C}$, for up to 8 reflows.

The fatigue failures were dominated by barrel cracking, generally in the mid-part of the barrel. Micro-sectioning of failed vias highlighted heavy concertina-like collapsing of barrels, and fatigue cracks through the plated copper walls. These failures were mostly in vias where the stress during reflow was highest (i.e. materials with a high z-axis, high aspect ratio vias, and/or high number of reflow profiles). Electroless nickel and immersion gold (ENIG) finishes were used, and the results show that the electroless nickel was significantly stronger than the copper. In many cases in which copper failures occurred the nickel remained intact.

Clear differences in performance were noted between the four laminates; phenolic materials were better than the dicy-cured laminates. All were sensitive to the peak reflow temperature and the number of passes. The z-axis CTE was a better indicator of susceptibility than T_g , for example, it was observed that high T_g and high z-axis CTE samples failed before low T_g and low CTE laminates. The higher the via aspect ratio, the greater was the susceptibility to failure.

Failure was monitored as a loss in electrical continuity of the daisy via chains. The electrical resistance was monitored either periodically (every 500 cycles) or continuously with an event detector having a 200nsec response time. The continuous monitoring detected failures at an earlier stage, typically at 50% to 75% of the fatigue life for the first failures for periodic monitoring. This is thought to be related to contraction effects closing fatigue cracks during continuous monitoring - periodic monitoring is carried out only at room temperature.

© Crown copyright 2007
Reproduced with the permission of the Controller of HMSO
and Queen's Printer for Scotland

ISSN 1754-2979

National Physical Laboratory
Hampton Road, Teddington, Middlesex, TW11 0LW

Extracts from this report may be reproduced provided the source is acknowledged and the extract is not taken out of context.

Approved on behalf of the Managing Director, NPL,
by Dr M G Cain, Knowledge Leader, Materials Team
authorised by Director, Industry and Innovation Division

CONTENTS

1	INTRODUCTION	1
2	METHODOLOGY:	2
2.1	TEST BOARD	2
2.2	TEST BOARD MATERIALS TYPES	3
2.3	CONDITIONING OF TEST BOARDS	3
2.4	Z-AXIS CO-EFFICIENT OF THERMAL EXPANSION (CTE) MEASUREMENTS	5
2.5	DYNAMIC MECHANICAL ANALYSIS (DMA) OF TG	6
2.6	THERMAL GRAVIMETRIC ANALYSIS (TGA) OF DECOMPOSITION TEMPERATURE	6
2.7	SCANNING ACOUSTIC MICROSCOPY (SAM)	6
2.8	THERMAL CYCLING AND ELECTRICAL TEST	6
3	RESULTS	7
3.1	Z-AXIS CO-EFFICIENT OF THERMAL EXPANSION (CTE) MEASUREMENTS	7
3.1.1	Standard Tg Dicy Cured (SD) Material Results	7
3.1.2	Standard Tg Phenolic Cured (SP) Material Results	8
3.1.3	High Tg Dicy Cured (HD) Material Results	9
3.1.4	High Tg Phenolic Cured (HP) Material Results	10
3.2	DYNAMIC MECHANICAL ANALYSIS (DMA) OF GLASS TRANSITION TEMPERATURE (TG)	11
3.3	THERMAL GRAVIMETRIC ANALYSIS (TGA) OF DECOMPOSITION TEMPERATURE	14
3.4	SCANNING ACOUSTIC MICROSCOPY	16
3.5	PERIODIC RESISTANCE MEASUREMENT DURING THERMAL CYCLING	16
3.6	CONTINUITY MONITORING DATA	19
4	DISCUSSION	22
4.1	Z-AXIS CTE MEASUREMENTS	22
4.2	DYNAMIC MECHANICAL ANALYSIS OF TG	24
4.3	THERMAL GRAVIMETRIC ANALYSIS OF DECOMPOSITION TEMPERATURE	24
4.4	PERIODIC MONITORING THERMAL CYCLING	25
4.5	CONTINUITY MONITORING DATA	31
5	CONCLUSIONS	33
6	ACKNOWLEDGEMENTS	34
7	REFERENCES.....	35

1 INTRODUCTION

The requirement to comply with the European regulations in 2006 banning lead is driving the adoption of new materials both in PCB assembly and bare board manufacture. The electronics manufacturing industry has been using SnPb-based solders for electrical and electronic interconnection for more than 60 years and the European ban on lead effectively discards all that experience of the reliability of soldered assemblies. Many organisations, including NPL, are working to improve the knowledge and experience of lead-free processing reliability, but many questions are still unanswered.

The alloy traditionally used for soldering in electronics manufacture has been changed from SnPb, and the preferred choice is a tin/silver/copper alloy, which has a higher melting point of approximately 217°C. Several workers have reported concerns that the increased processing temperatures associated with these new alloys, may affect the reliability of the printed circuit substrate. In consequence, this project was developed to study any reduction in the reliability of substrates during and after the transition to a completely lead-free assembly process.

The replacement solders for tin-lead are all high tin alloys with significantly higher melting points than conventional tin-lead materials. Substrate technology has been developed around reinforced resin materials, and any degradation at the higher process temperatures required by the new alloys, may be an issue. Reliability of plated-through holes and micro-vias may be degraded, the propensity for multi-layer substrates to delaminate may be increased, and electrical insulation properties may be disrupted, due to increased breakdown by cathodic or anodic electro-migration.

These factors are compounded by the closer proximity of the conducting elements, necessitated by miniaturisation-driven advances. The removal of non-functional pads to facilitate signal routing and improve drilling of fine vias, may also affect substrate reliability at lead-free soldering temperatures.

The objectives of this joint DTI/industry project were:

- To provide the electronics manufacturing industry with a test method and data to measure the effect of the higher temperatures associated with lead-free soldering on the reliability of electronics substrate structures.
- To improve industry confidence in the reliability of PCB substrates during and after the change over to lead-free solders.

This report covers Phase 1 of the project, which comprised an initial assessment of PCB reliability after lead-free processing and an evaluation of the comparative performance of interconnection stress testing (IST) and thermal cycle testing.

Phase 1 was based on three aspects:

- The effect of via pitches and aspect ratios for through-holes and micro-vias
- The effect of lead-free processing on PCB reliability including via performance, delamination and electrical isolation properties
- An evaluation of the relative performance of IST and thermal cycle testing

2 METHODOLOGY:

2.1 TEST BOARD

A test panel was designed that included seven coupons with various features, and is shown in Figure 1. The board was a 2.5mm thick, 10 layer structure with an electroless nickel/immersion gold (ENIG) finish. The overall size was 300mm x 200mm. The letters on the image designate the different test coupons as follows:

- A - 10:1, 8:1, 6:1 and micro-vias for thermal cycling
- B - 8:1 vias for thermal shock testing
- C - 6:1 vias for interconnection stress testing
- D - 8:1 vias for interconnection stress testing
- E - 8:1 vias for interconnection stress testing
- F - 10:1 vias for interconnection stress testing
- G - 8:1 for delamination testing

Hence a 10:1 via in a 2.5mm board has a finished diameter of 250 μ m. The via-chain patterns were identical for both the thermal cycling coupon and the IST coupons reported in Ref 1.

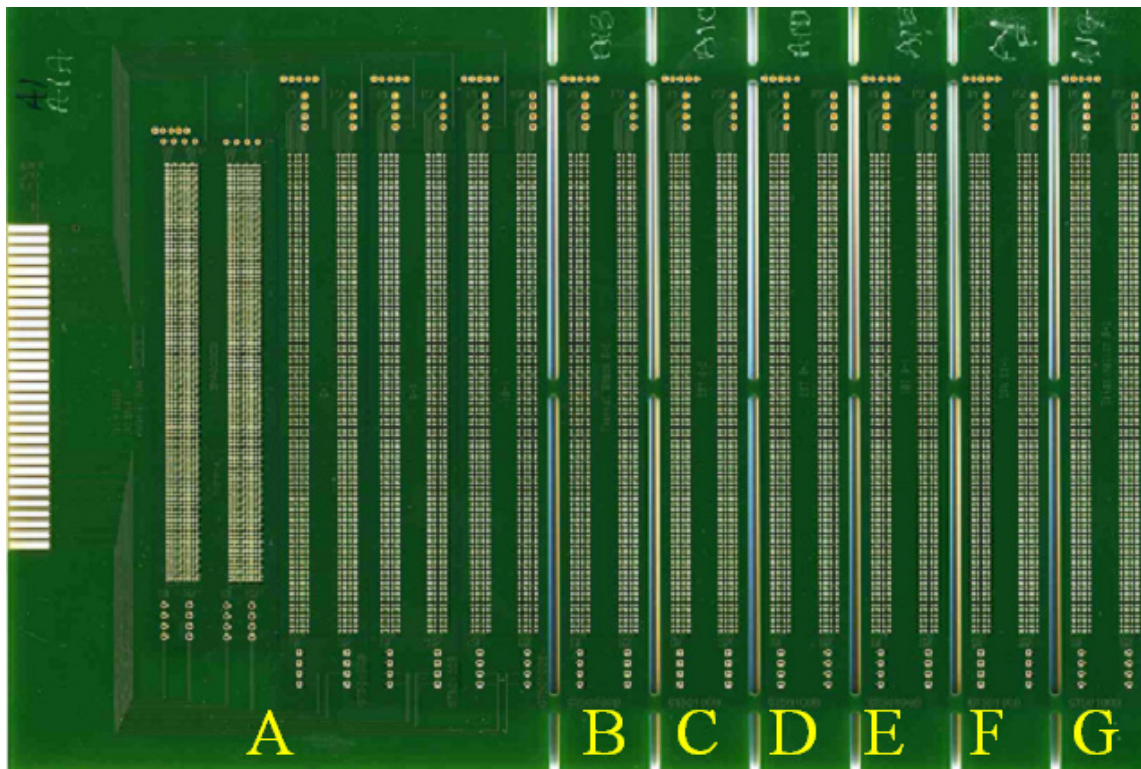


Figure 1: Test board showing individual test patterns

2.2 TEST BOARD MATERIALS TYPES

Four different basic laminate types from a single supplier were chosen for phase 1. These were:

- SD - A standard glass transition temperature (Tg) material, dicy cured, with a Tg of ~140°C
- SP - A standard Tg material, phenolic cured with a Tg ~150°C
- HD - A high Tg material, dicy cured with a Tg ~170°C
- HP - A high Tg material, phenolic cured with a Tg ~170°C

2.3 CONDITIONING OF TEST BOARDS

To determine the effects of lead-free reflow soldering on the reliability of the PCBs, test boards were reflowed in a 10-zone reflow oven with three different profiles representing peak reflow temperatures of 230, 245 and 260°C, and molten solder times between 1min and 1min 25seconds. These profiles are illustrated in Figures 2 to 4. The PCBs were reflowed up to 8 times, with the boards allowed to cool for 15 minutes before being re-profiled. Profiling was halted after 8 reflows as the HD material samples blistered. A summary of the conditioning undertaken is given in Table 1.

Table 1: Summary of Reflow Conditioning

Batch	Laminate Type	Peak Reflow Temp	No. of Passes
A	High Tg phenolic cured (HP)	260 °C	3
B	High Tg phenolic cured (HP)	260 °C	6
C	High Tg phenolic cured (HP)	260 °C	8
D	Standard Tg dicy cured (SD)	260 °C	6
E	Standard Tg dicy cured (SD)	245 °C	6
F	Standard Tg dicy cured (SD)	230 °C	6
G	Standard Tg phenolic cured (SP)	260 °C	6
H	High Tg dicy cured (HD)	260 °C	6
J	Standard Tg dicy cured (SD)	260 °C	3
K	Standard Tg dicy cured (SD)	260 °C	8

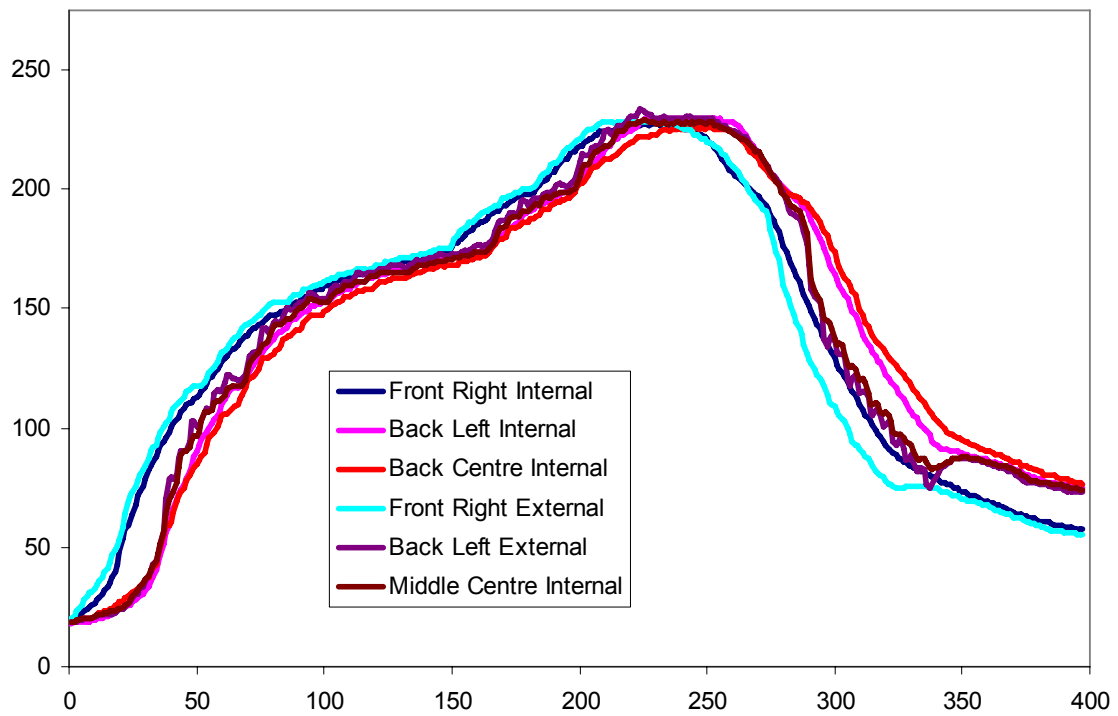


Figure 2: Thermal profile with 230 °C peak temperature

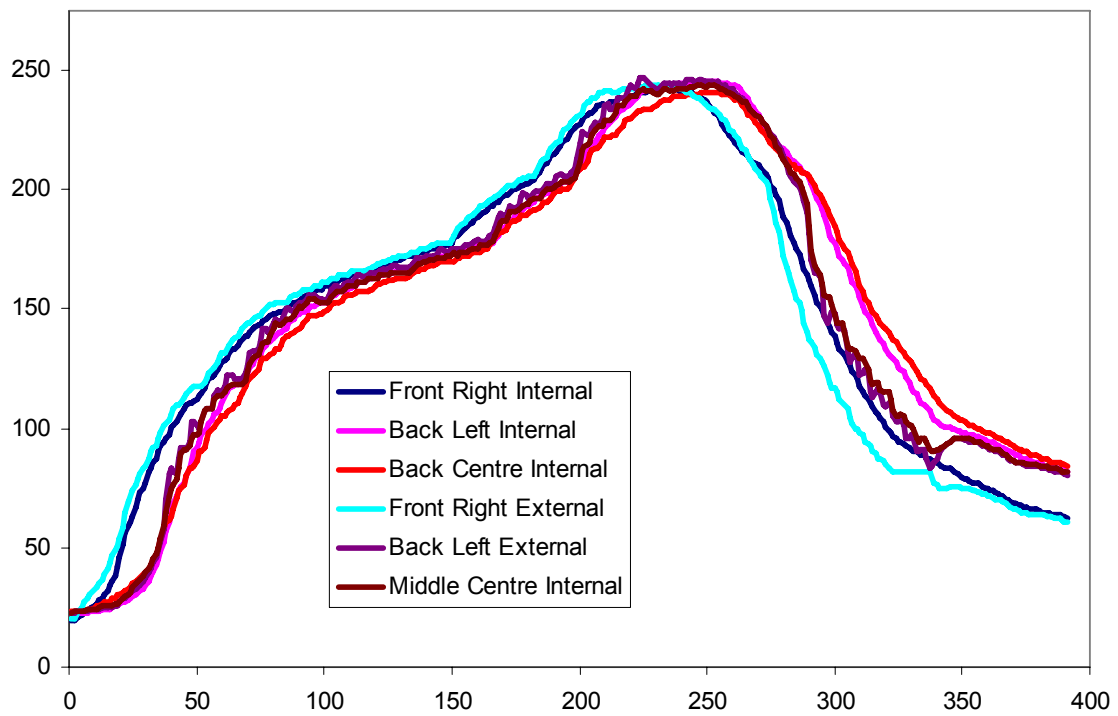


Figure 3: Thermal profile with 245 °C peak temperature

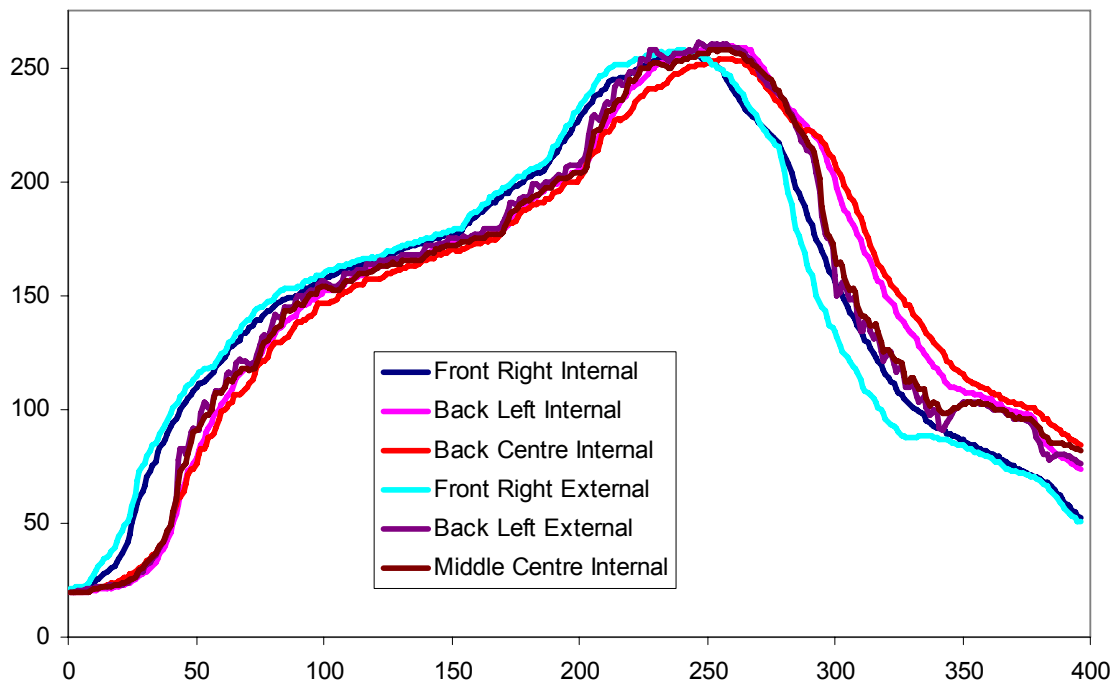


Figure 4: Thermal profile with 260 °C peak temperature

2.4 Z-AXIS CO-EFFICIENT OF THERMAL EXPANSION (CTE) MEASUREMENTS

The CTE measurements were undertaken using a calibrated Linseis alumina dilatometer (Figure 5) on a stack of six 6mm x 6mm coupons. The temperature range of the CTE measurements was varied from room temperature to 250 °C. The measurements were repeated three times: the first cycle allows for annealing effects, and any settling and bedding-in effects in response to the heating cycle. Averaged expansion coefficients were then computed for the second and third cycles. A 1 °C/min heating and cooling rate was used to a maximum temperature of about 185 °C, with no hold at the peak temperature. The tests were conducted on as-manufactured material (i.e. before profiling). For the SD material, measurements were also undertaken after 6 reflow profiles at 260 °C.



Figure 5: Dilatometer equipment used for measuring z-axis CTE

2.5 DYNAMIC MECHANICAL ANALYSIS (DMA) OF TG

DMA measurements were undertaken (Ref: 2) on a TA Instruments DMA 2980 machine according to IPC-TM-650 2.4.24.2 in single cantilever bending mode. The heating rate was 2°C/min with the tests being conducted on as-manufactured material (i.e. before profiling). Based on research undertaken by NPL in collaboration with industry (Ref: 2), the inflection point in the storage modulus curve is the preferred point (Ref: 3) for T_g analysis.

2.6 THERMAL GRAVIMETRIC ANALYSIS (TGA) OF DECOMPOSITION TEMPERATURE

TGA provides a measure of the mass loss during a temperature ramp in a furnace. Tests conducted in this work were undertaken according to ASTM D3850 (Ref: 4), using as-manufactured material (i.e. before profiling)

2.7 SCANNING ACOUSTIC MICROSCOPY (SAM)

SAM images were acquired using a SONIX Scanning Acoustic Microscope.

2.8 THERMAL CYCLING AND ELECTRICAL TEST

Thermal cycling was carried out in a single chamber system, up to 3000 cycles, -55 to 125 °C, with 5min dwells, ramps of 10°C per minute, giving a total cycle time of ~ 1 hour.

Thermal cycling was undertaken on coupon A, which consisted of two chains each of 10:1, 8:1 and 6:1 through-vias, and two chains of micro-vias connected to edge connectors so that the resistance of the chains could be monitored.

During the thermal cycling periodic electrical monitoring was undertaken on all PCBs at regular intervals. Boards were removed from the thermal cycling oven for the periodic monitoring and inserted into an edge connector of the switching system and DVM. Failure was considered to be an increase in resistance to above 100 Ω .

A limited number of circuits were continuously monitored electrically in the chamber by connection to event detectors. The latter registered a failure when the chain resistance increased to > 5k Ω for a period greater than 200ns. Continuous monitoring was undertaken on batches B, D, F, G and H.

3 RESULTS

3.1 Z-AXIS CO-EFFICIENT OF THERMAL EXPANSION (CTE) MEASUREMENTS

3.1.1 Standard Tg Dicy Cured (SD) Material Results

The results of the Z-axis measurements for this material are given in Table 2 with a typical graphical representation in Figure 6. For the SD material, measurements were taken before and after conditioning using the 260°C peak reflow profile for 6 reflows.

Table 2: Z-axis CTE results for SD materials

Range	Before Profiling	After Profiling
	CTE (ppm/degC)	CTE (ppm/degC)
50-120°C	70	68
160-180 °C	337	347
180-160 °C	357	351
120 to 50 °C	78	76

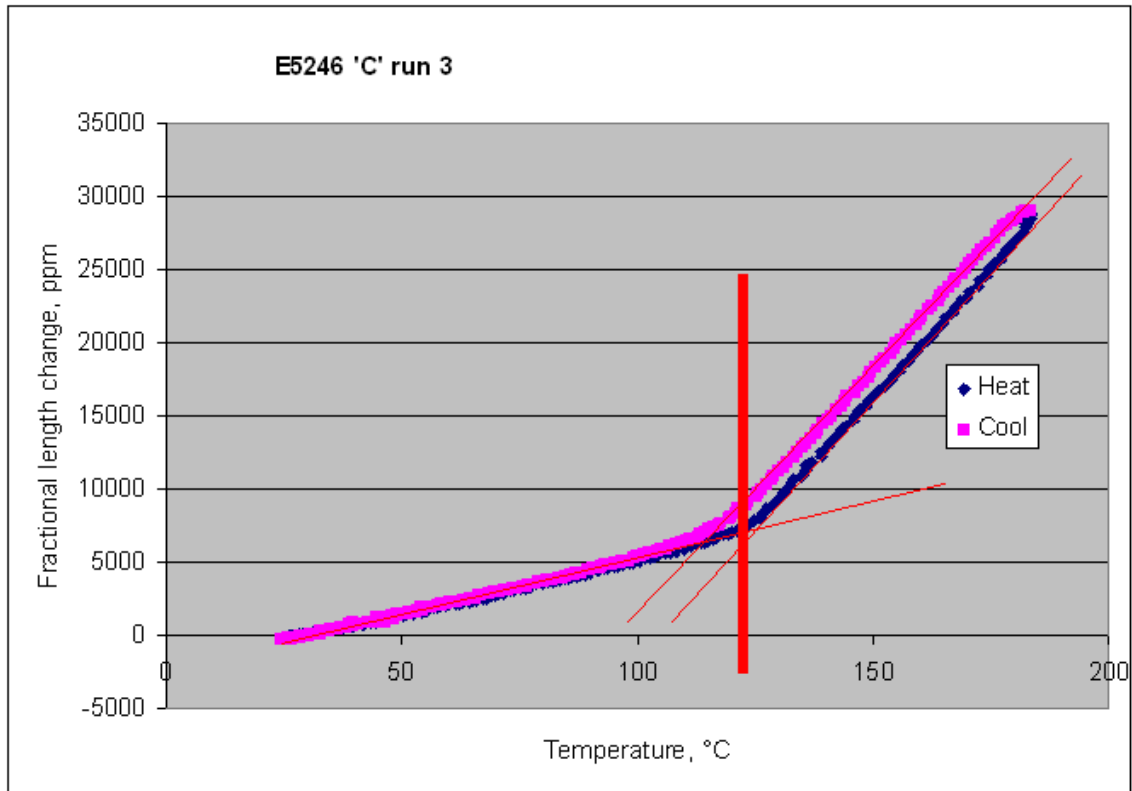


Figure 6: Typical dilatometer results for SD material before profiling

3.1.2 Standard Tg Phenolic Cured (SP) Material Results

The results of the Z-axis measurements for this material in the as-received condition are given in Table 3 with a typical graphical representation in Figure 7.

Table 3: Z-axis CTE results for SP materials

Range	CTE (ppm/degC)
50-120°C	61
160-180 °C	274
180-160 °C	288
120 to 50 °C	65

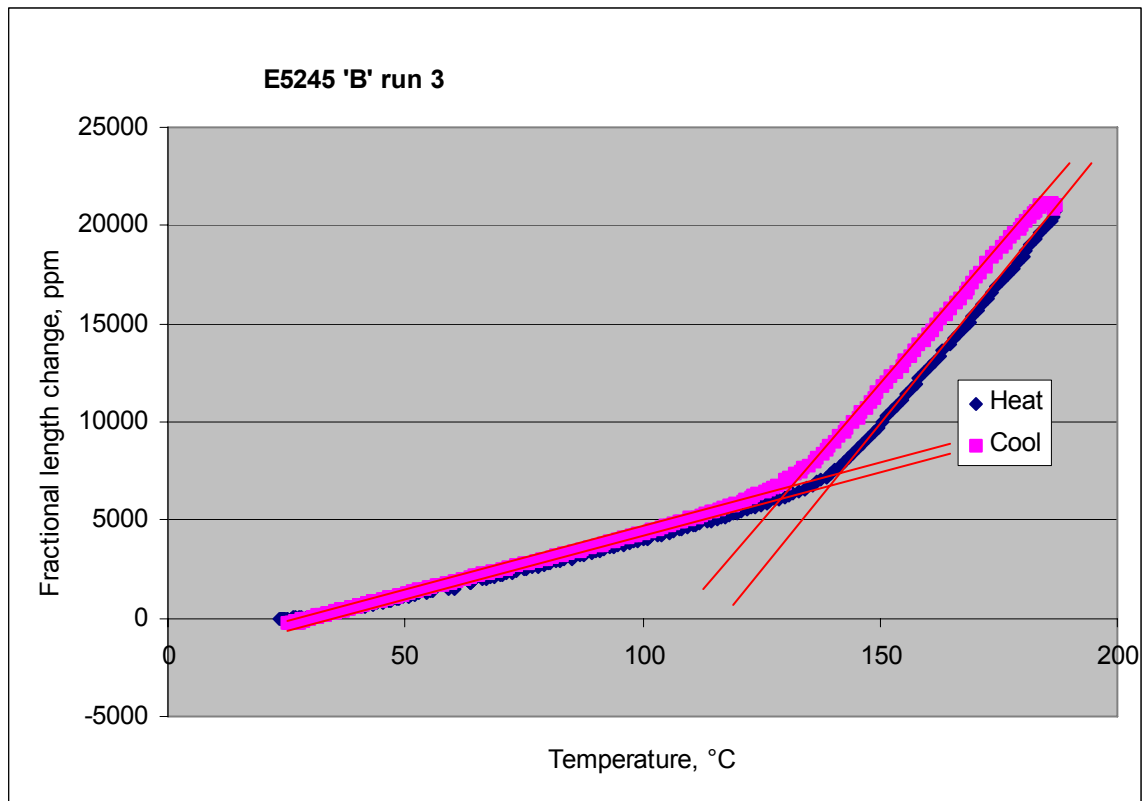


Figure 7: Typical dilatometer results for SP material

3.1.3 High Tg Dicy Cured (HD) Material Results

The result of the Z-axis measurements for this material in the as-received condition are given in Table 4 with a typical graphical representation in Figure 8.

Table 4: Z-axis CTE results for HD materials

Range	CTE(ppm/degC)
50-120°C	69
160-180 °C	290
180-160 °C	313
120 to 50 °C	69

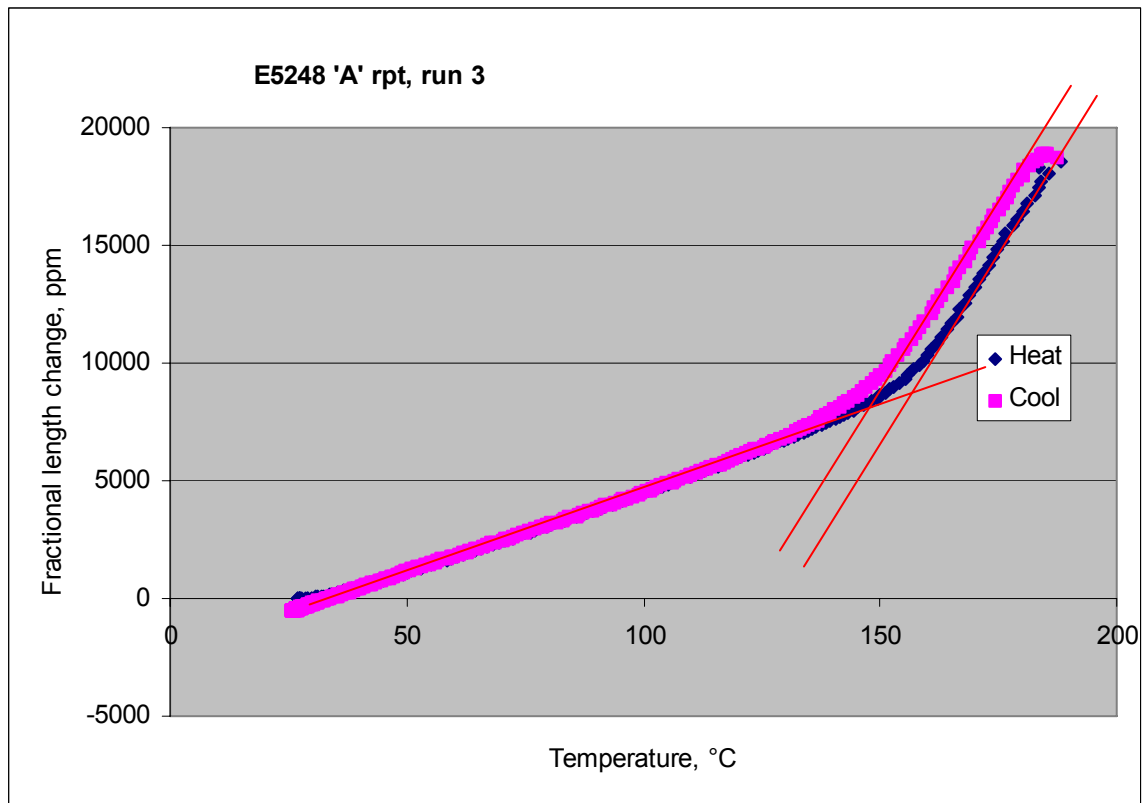


Figure 8: Typical dilatometer results for HD material

3.1.4 High Tg Phenolic Cured (HP) Material Results

The results of the Z-axis measurements for this material are given in Table 4 with a typical graphical representation in Figure 9. For the HP material, measurements were taken before and after conditioning using the 260°C peak reflow profile for 6 reflows.

Table 5: Z-axis CTE results for HP materials

Range	Before Profiling	After Profiling
	CTE (ppm/degC)	CTE (ppm/degC)
50-120°C	63	58
160-180 °C	248	231
180-160 °C	265	249
120 to 50 °C	64	62

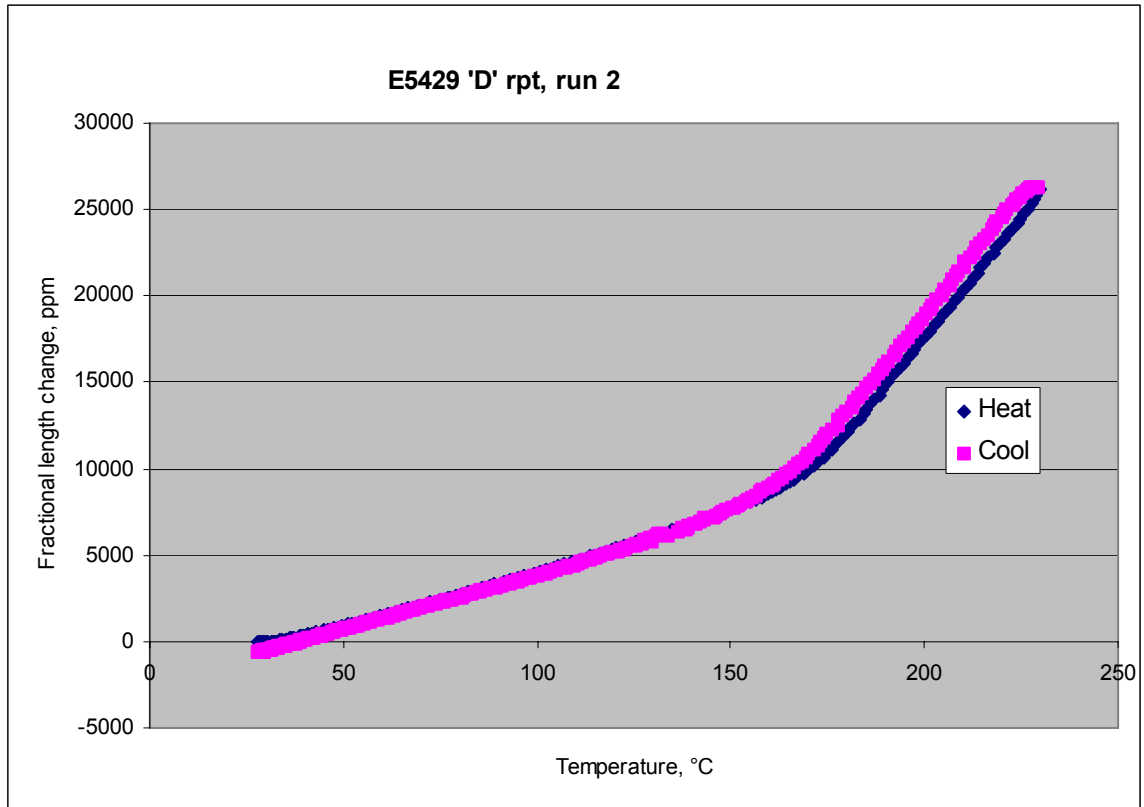


Figure 9: Typical dilatometer results for HP material

3.2 DYNAMIC MECHANICAL ANALYSIS (DMA) OF GLASS TRANSITION TEMPERATURE (TG)

The results of the DMA Tg analyses are given in Table 6 with the full plots for each material in the as-received condition, presented in Figures 10 to 13. The preferred method of determining Tg is the inflection point in the storage modulus.

Table 6: The results of Tg Analyses

Material	Storage modulus °C	Loss modulus peak °C	Tan delta peak °C
SD	136.8	136.9	140.8
SP	149.9	150.3	154.7
HD	171.9	172.1	176.9
HP	174.4	175.4	180.9

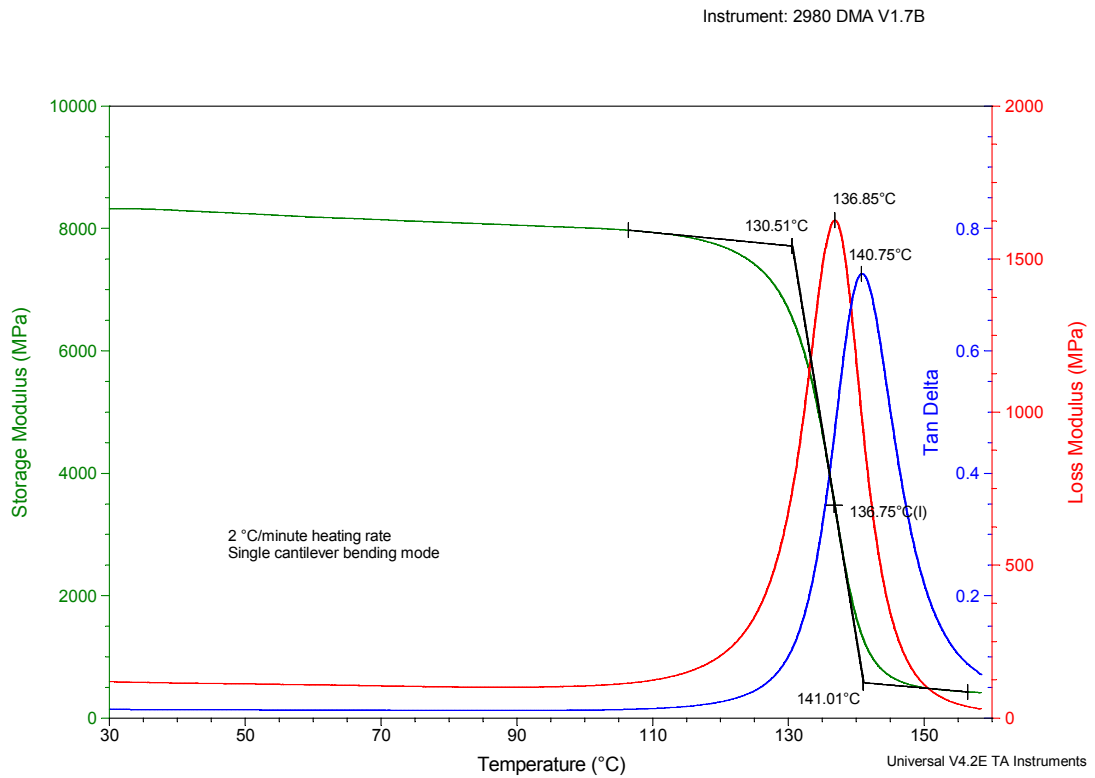


Figure 10: Typical DMA results for SD material

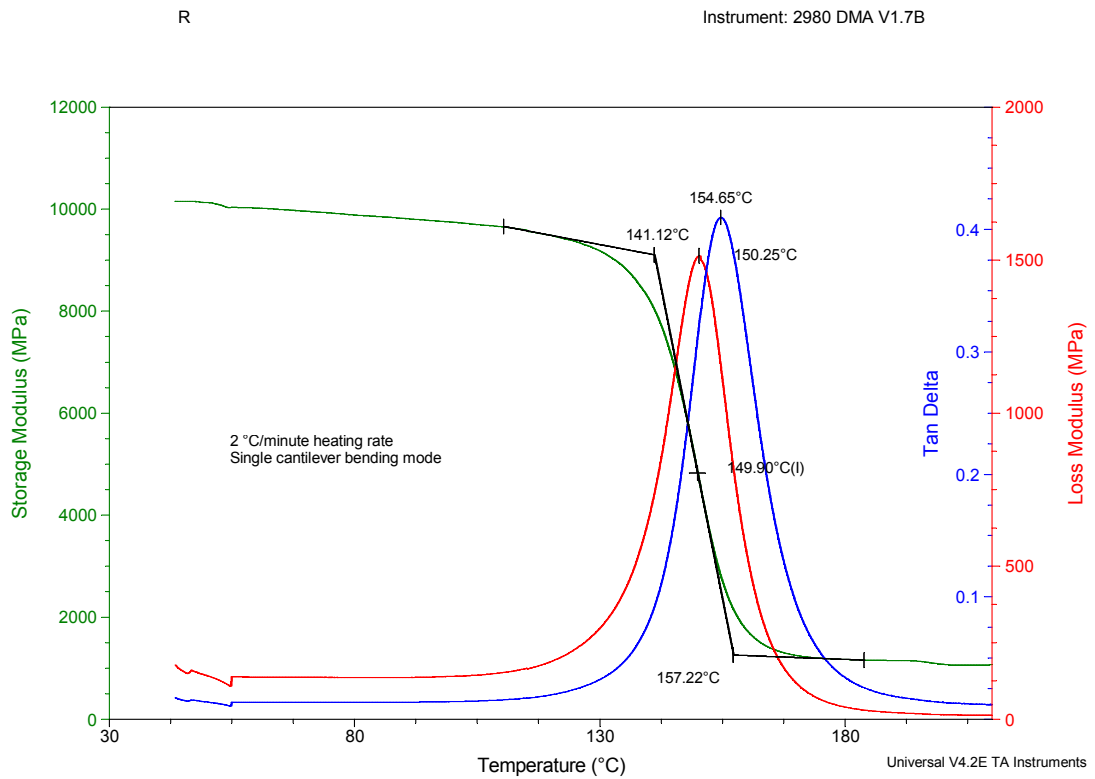


Figure 11: Typical DMA results for SP material

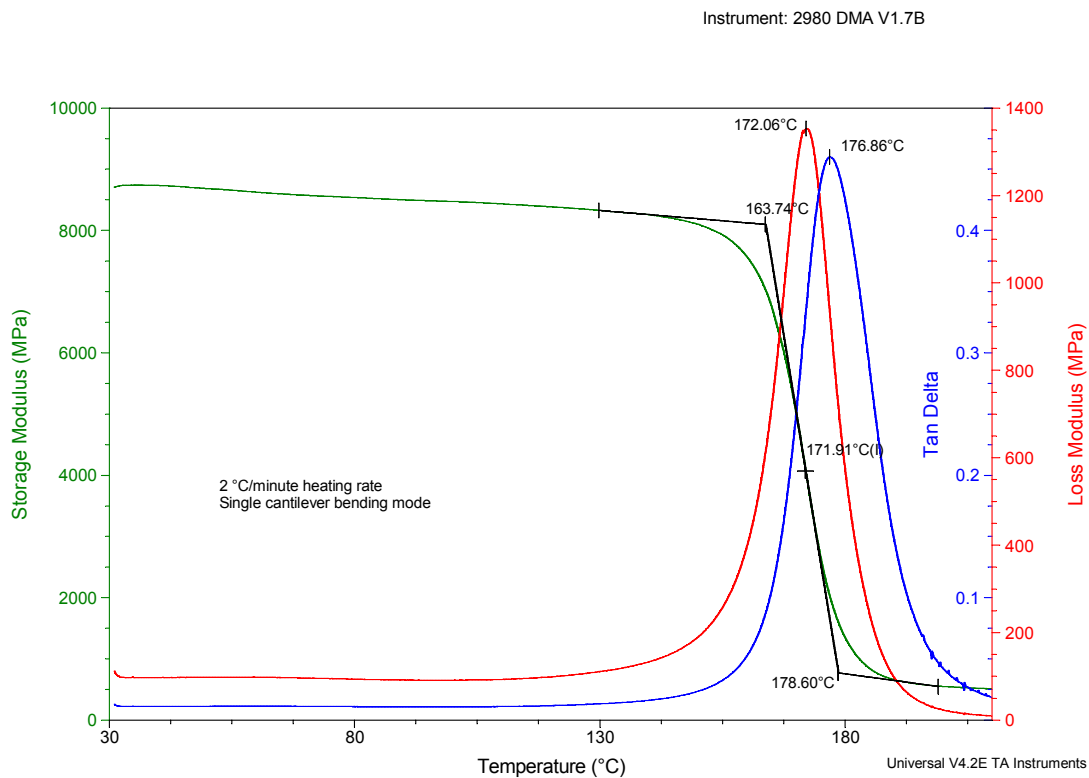


Figure 12: Typical DMA results for HD material

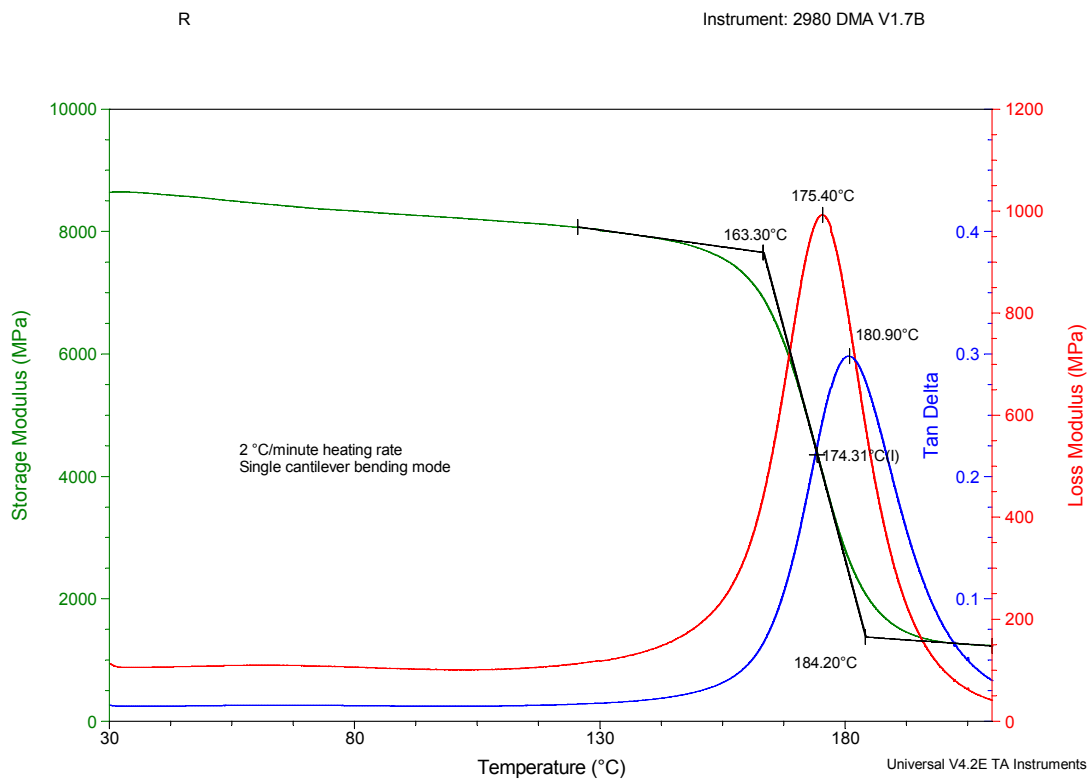


Figure 13: Typical DMA results for HP material

3.3 THERMAL GRAVIMETRIC ANALYSIS (TGA) OF DECOMPOSITION TEMPERATURE

The decomposition temperature (T_d) was calculated as the point at which a 5% weight loss had occurred. A summary of the measured values is given in Table 7, and examples of TGA scans are represented in Figures 14 to 17.

Table 7: Measured decomposition temperature

Material	Decomposition Temperature
SD	295°C
SP	310°C
HD	295°C
HP	315°C

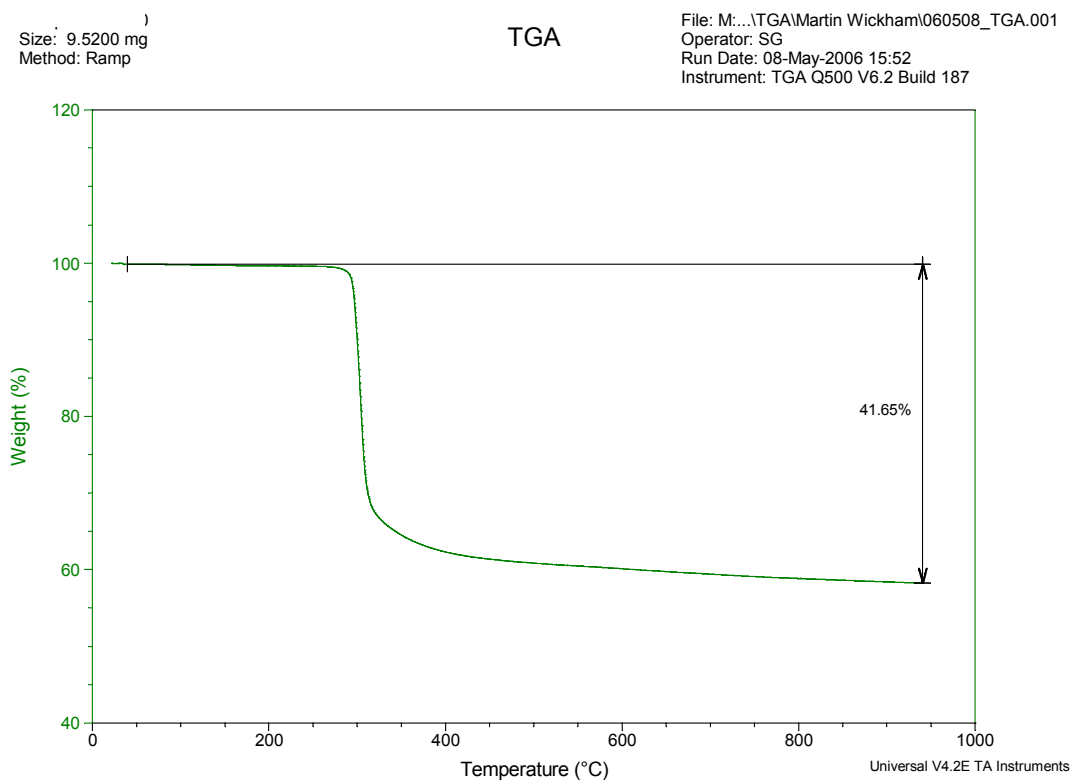


Figure 14: Typical TGA scan for SD material

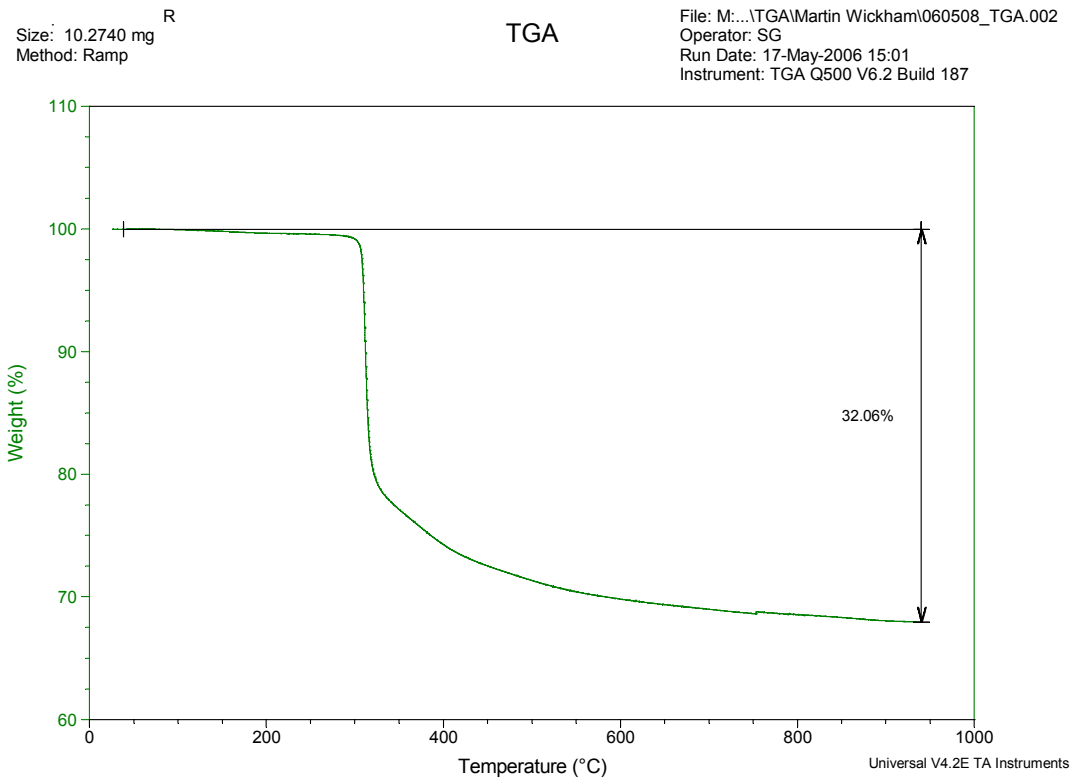


Figure 15: Typical TGA scan for SP material

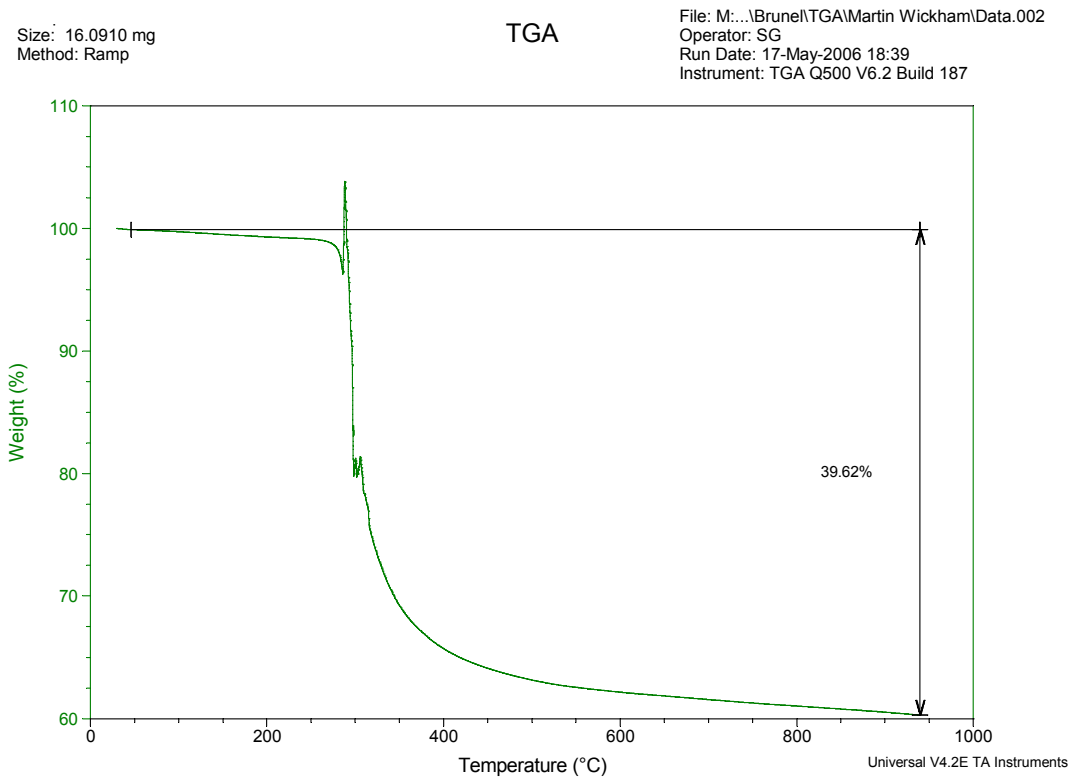


Figure 16: Typical TGA scan for HD material

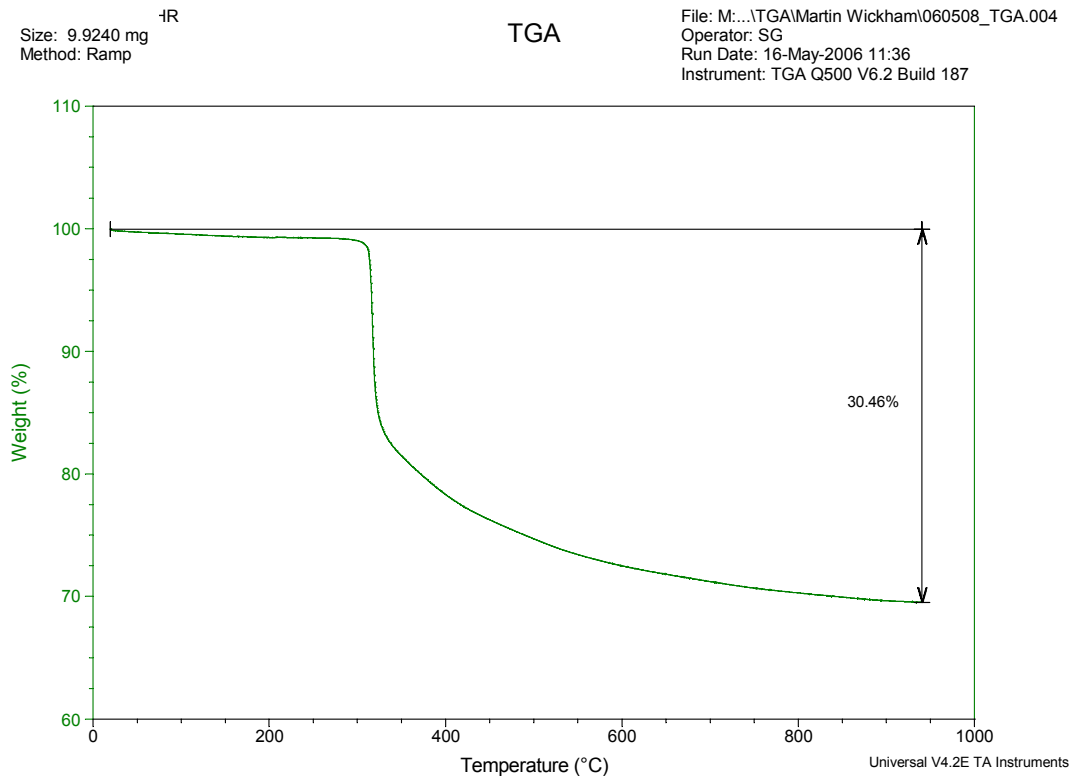


Figure 17: Typical TGA scan for HP material

3.4 SCANNING ACOUSTIC MICROSCOPY

SAM and enhanced SAM images of a blistered HD material PCB after 6 profiles at 260 °C (see Figure 18) were complex and unsuitable for investigation of delamination.

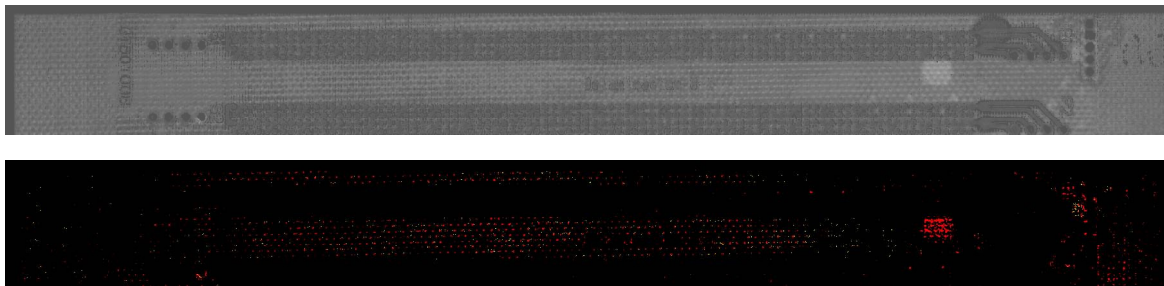


Figure 18: SAM and enhanced SAM images of HD material after 6 profiles at 260°C

3.5 PERIODIC RESISTANCE MEASUREMENT DURING THERMAL CYCLING

Cumulative electrical failure development for samples up to 3000 thermal cycles, and for a range of materials for 10:1, 8:1 and 6:1 through vias and micro-vias, is summarised in Figures 19 to 22. The coding used for these samples were given in Table 8.

Table 8 : Thermal cycling electrical failure codes

Code	Variable
SD	Standard Tg, dicy cured material
SP	Standard Tg, phenolic cured material
HD	High Tg, dicy cured material
HP	High Tg, phenolic cured material
L	230°C peak reflow
M	245°C peak reflow
H	260°C peak reflow
3	3 profiles
6	6 profiles
8	8 profiles
W	6:1 aspect ratio
M	8:1 aspect ratio
T	10:1 aspect ratio
U	micro-via
S	sense circuit

Thus SDH8TS refers to:

- SD – standard Tg, dicy-cured material (see Section 2.2)
- H – 260°C peak reflow
- 8 – 8 reflows
- T – 10:1 through-vias
- S – sense circuit of test pattern

All resistance measurements were undertaken on the sense circuits of the via chains, these being daisy chains through the complete via.

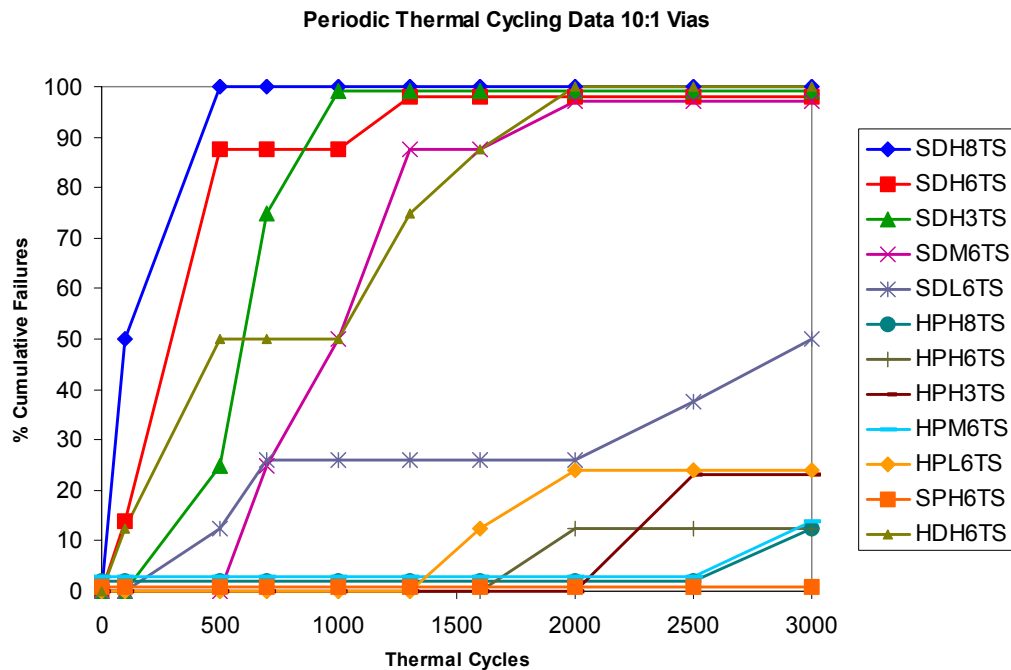


Figure 19: Cumulative periodic electrical test failures during thermal cycling for 10:1 vias, for four material types (SD, HP, SP & HD), three conditioning Profiles (230, 245 & 260°C), and for 3, 6 and 8 reflows

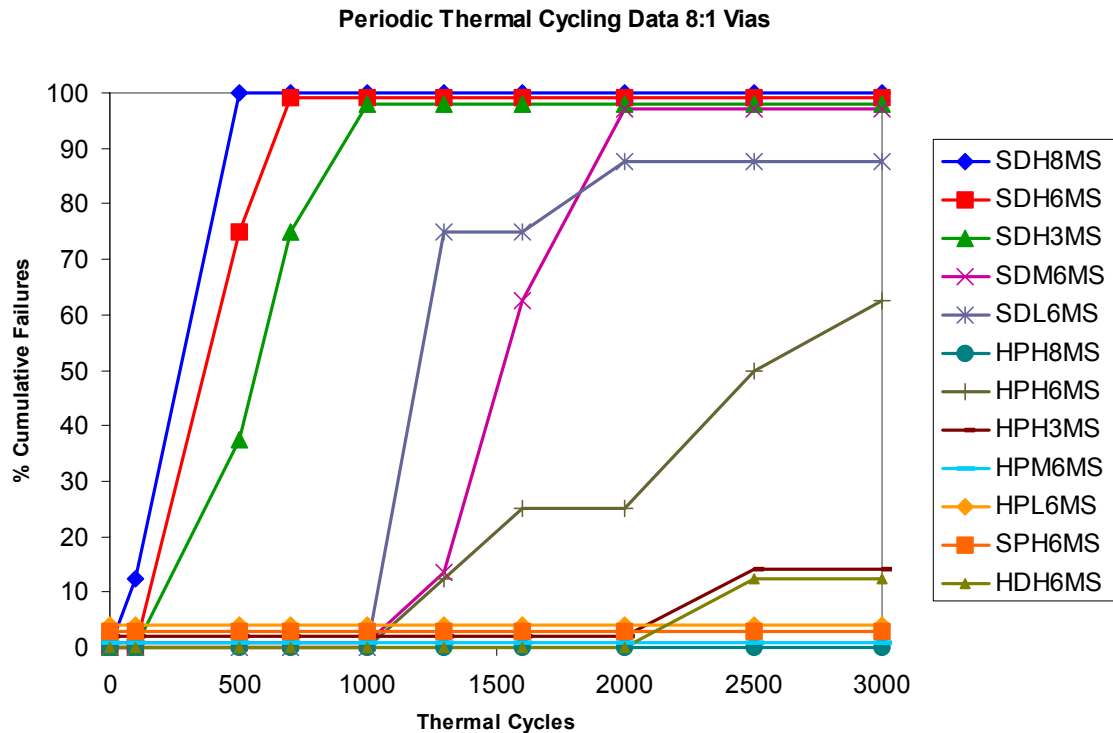


Figure 20: Cumulative periodic electrical test failures during thermal cycling for 8:1 vias, for four material types (SD, HP, SP & HD), three conditioning profiles (230, 245 & 260°C) and for 3, 6 and 8 reflows

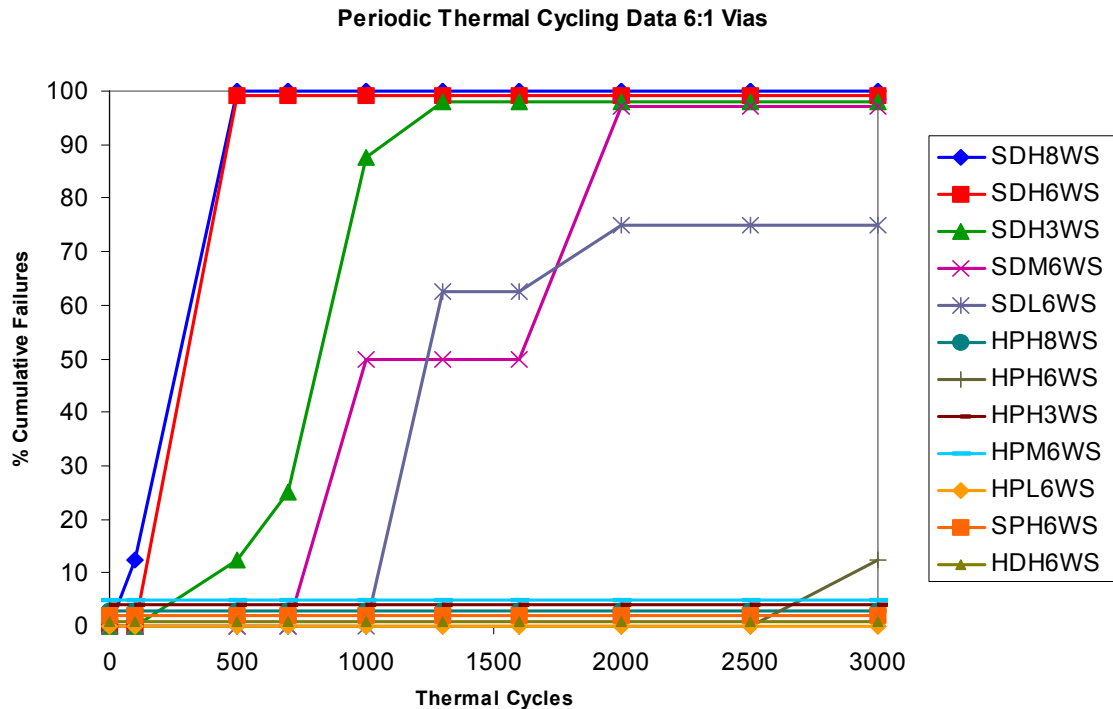


Figure 21: Cumulative periodic electrical test failures during thermal cycling for 6:1 vias, for four material types (SD, HP, SP & HD), three conditioning profiles (230, 245 & 260°C) and for 3, 6 and 8 reflows

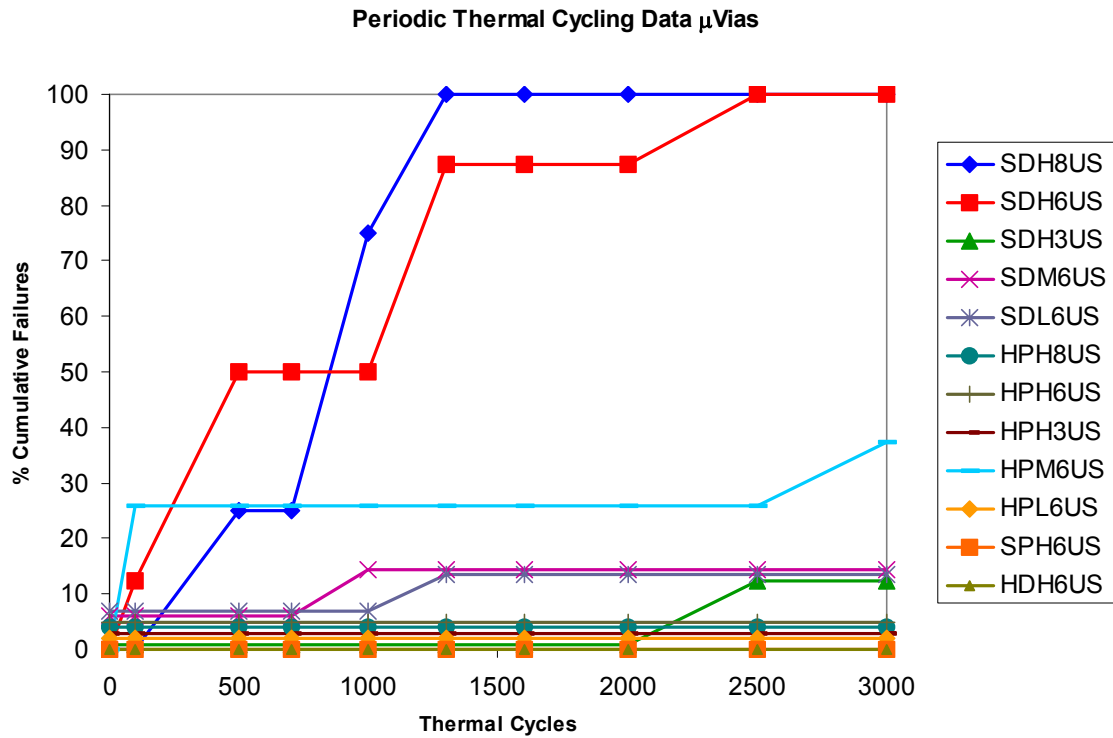


Figure 22: Cumulative periodic electrical test failures during thermal cycling for micro-vias, for four material types (SD, HP, SP & HD), three conditioning profiles (230, 245 & 260°C) and for 3, 6 and 8 reflows

3.6 CONTINUITY MONITORING DATA

Cumulative electrical failure development for samples up to 3000 thermal cycles, and for a range of materials for 10:1, 8:1 and 6:1 through-vias, is summarised in Figures 23 to 27. The codes for these samples were as given in Table 8 above. It should be noted that whilst all HDH6TS samples failed before 143 cycles, none of the SPH6MS, SPH6WS, HDH6WS and HPH6WS coupons failed before 3000 cycles were completed.

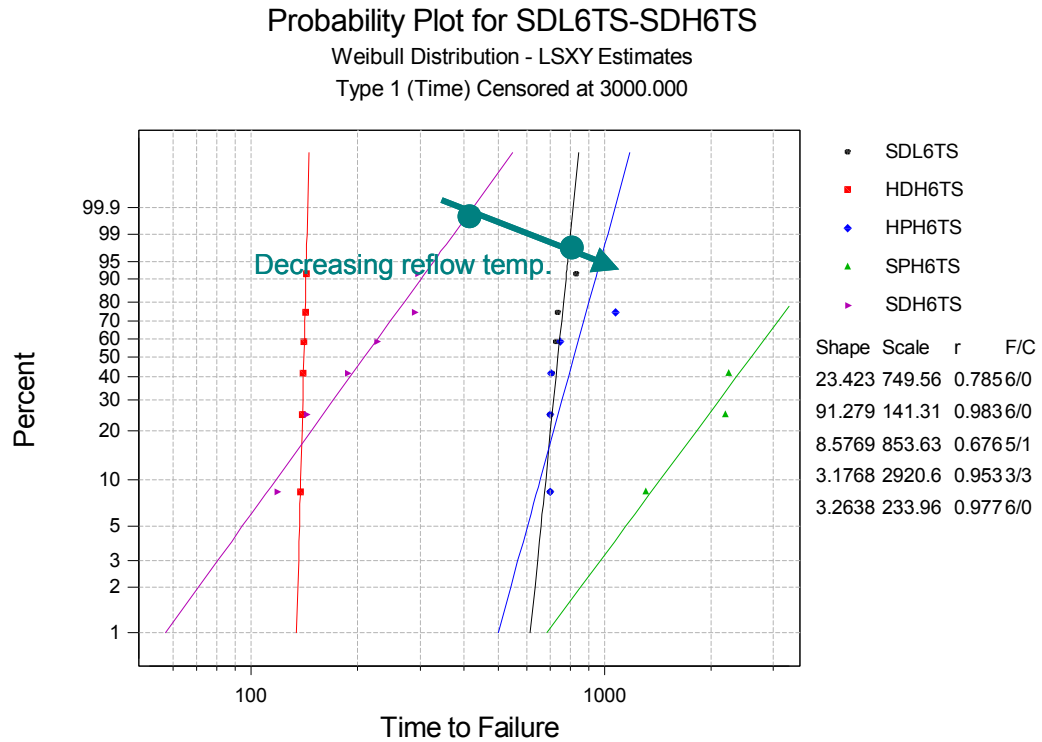


Figure 23: Cumulative continuity monitoring electrical test failures during thermal cycling for 10:1 vias, for four material types (SD, HP, SP & HD), two conditioning profiles (230 & 260°C) and for 6 reflows

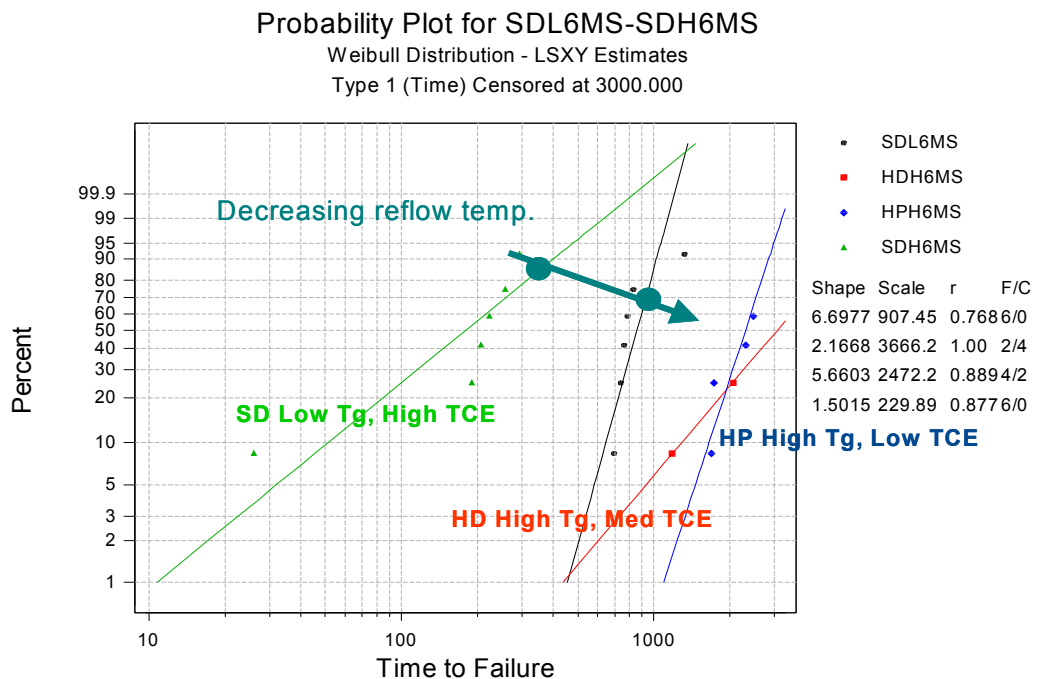


Figure 24: Cumulative continuity monitoring electrical test failures during thermal cycling for 8:1 vias, for four material types (SD, HP, SP & HD), two conditioning profiles (230 & 260°C) and for 6 reflows

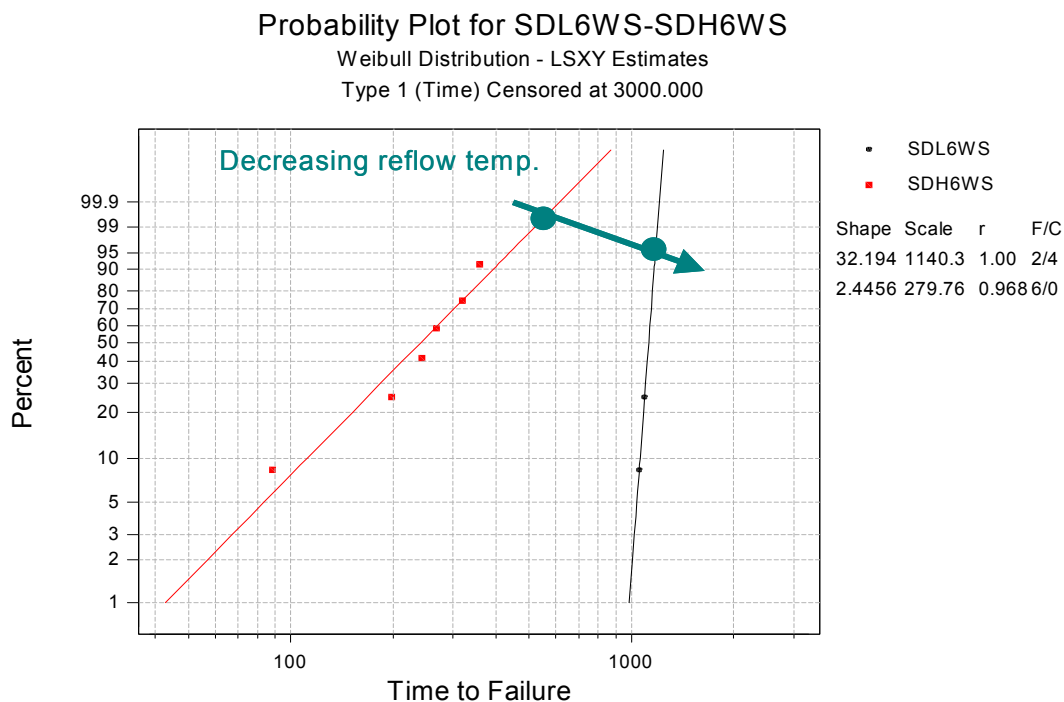


Figure 25: Cumulative continuity monitoring electrical test failures during thermal cycling for 6:1 vias, for SD material, two conditioning profiles (230 & 260°C) and for 6 reflows

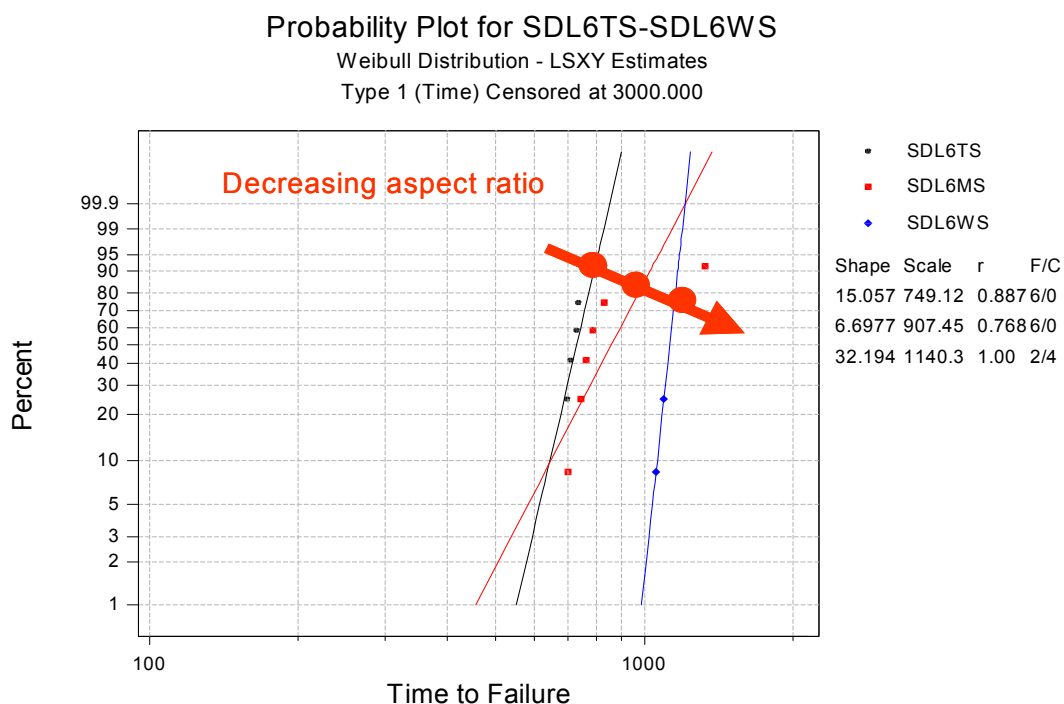


Figure 26: Cumulative continuity monitoring electrical test failures during thermal cycling for 10:1, 8:1 and 6:1 vias, for SD material, 230°C conditioning profile and for 6 reflows

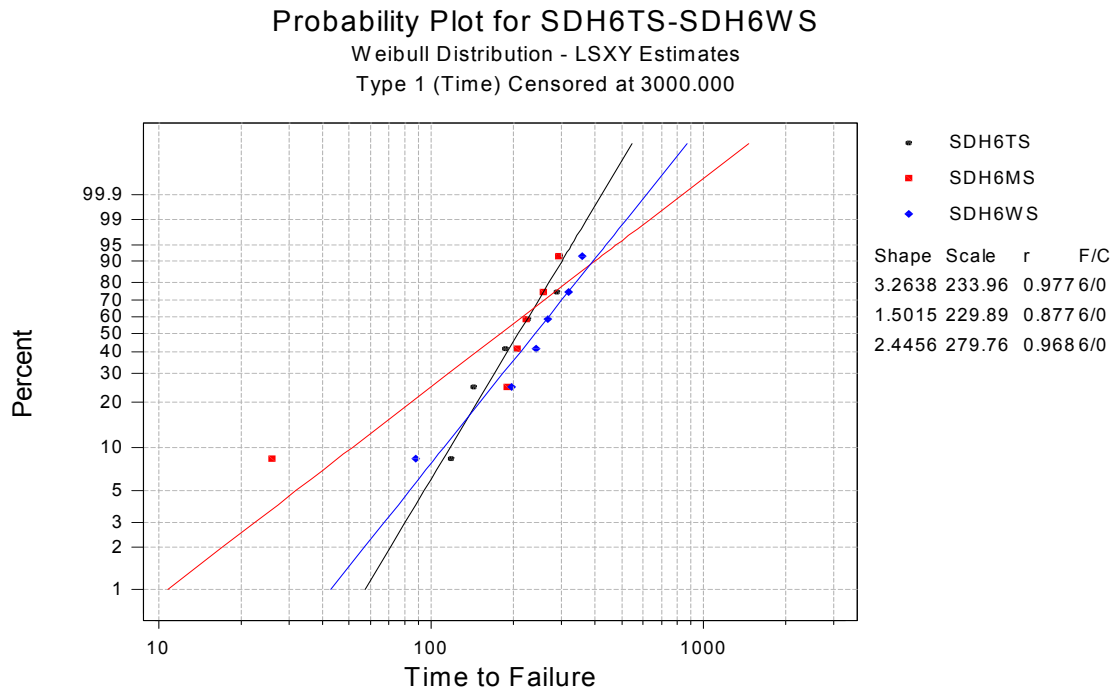


Figure 27: Cumulative continuity monitoring electrical test failures during thermal cycling for 10:1, 8:1 and 6:1 vias, for SD material, 260°C conditioning profile, and for 6 reflows

4 DISCUSSION

4.1 Z-AXIS CTE MEASUREMENTS

A comparison between the measured CTE values and typical values quoted by the laminate supplier is given in Table 9. In all cases, the measured CTEs were above the manufacturers' quoted values. Whilst the CTEs were typically 20ppm above the quoted values for materials measured below T_g , the difference varied between 10 and 100ppm for materials measured above T_g . The CTEs above T_g were in the range 256 to 347 ppm/degC. Significantly higher measured values were obtained from the two dicy-cured materials (SD/HD), with the SD material having a 39% higher value than the HP material. It should be noted that the manufacturers' values relate to the basic laminate, not the built multilayer board on which these measurements were made. The built board could involve different resin contents and glass styles to those taken by the laminate manufacturer.

Table 9: Comparison of measured CTE values and the typical values quoted by the laminate supplier (ppm/°C)

		SD	SP	HD	HP
50-120 °C	Measured	74	63	69	63
	Quoted Typical	50	45	50	45
160-180 °C	Measured	347	281	301	256
	Quoted Typical	250	270	250	220

The effect of these differences in CTE can clearly be seen in Figure 28, in which the expansion for the high CTE SD material is compared with that of the low CTE HP material. As the temperature of the PCB moves above the T_g of the base material, the higher z-axis of expansion of the SD material (36% higher than the HP material) will result in a greater stress on the barrel of the vias. Additionally, because the SD material has a lower T_g, this increased stress will occur for a longer period as indicated by the red area on the graph. Thus the SD material suffers doubly from a low T_g and high z-axis expansion above the T_g, leading to higher stressing of the vias during reflow soldering.

During thermal cycling, only the CTEs below the T_g are significant as the upper temperatures reached during the cycling are below the T_g of the materials in this study. Again the SD material had a high z-axis CTE as measured between room temperature and 125°C. On average this was 17% higher than the HP material and would again result in greater stress on the vias during thermal cycling. A comparison over the temperature range concerned is presented in Figure 29. It is also worth noting that the z-axis expansion for the HD material was also 10% higher than for the SP or HP materials.

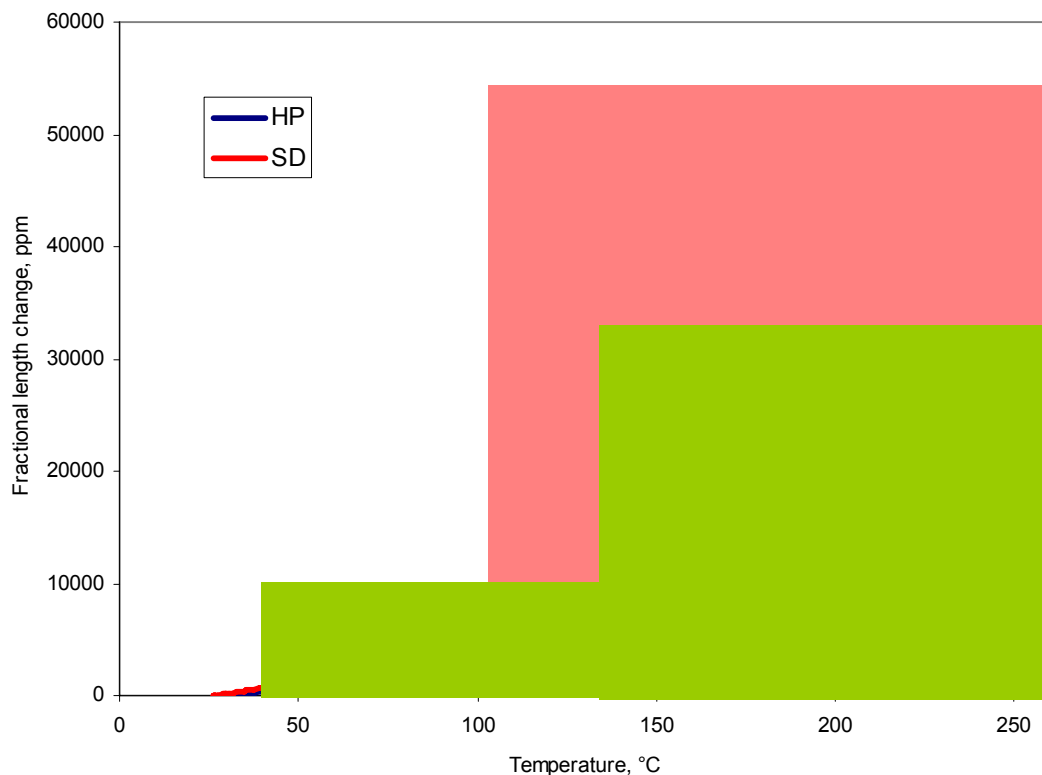


Figure 28: Comparison of expansion differences during reflow for SD (high CTE) and HP (low CTE) materials

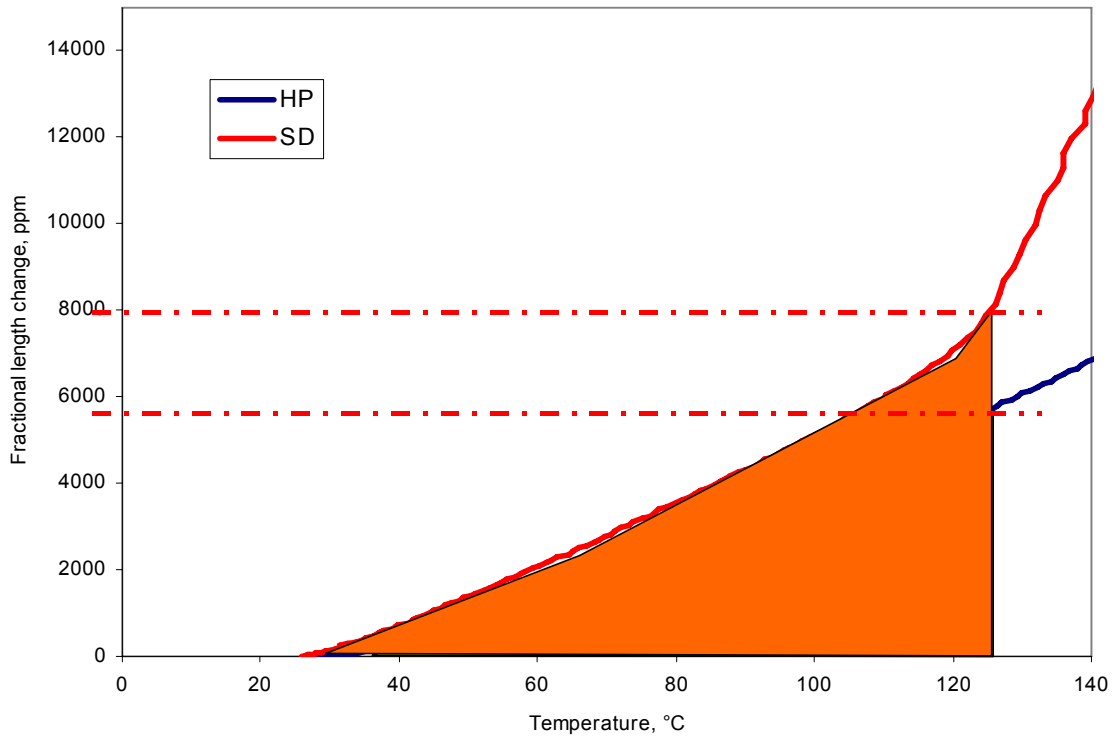


Figure 29: Comparison of expansion differences during thermal cycling for SD (high CTE) and HP (low CTE) materials

4.2 DYNAMIC MECHANICAL ANALYSIS OF TG

A comparison between measured values of T_g and supplier's quoted values (Table 10), indicates there is good agreement between the two sets of values.

Table 10: Comparison of measured T_g values by different parameters and the typical values quoted by the laminate supplier

Material	Storage modulus °C	Loss modulus peak °C	Tan delta peak °C	Typical suppliers quoted value
SD	136.8	136.9	140.8	140
SP	149.9	150.3	154.7	150
HD	171.9	172.1	176.9	175
HP	174.4	175.4	180.9	180

4.3 THERMAL GRAVIMETRIC ANALYSIS OF DECOMPOSITION TEMPERATURE

A comparison between measured values of T_d and supplier's quoted typical values (Table 11) indicates that the measured values are lower than the quoted values. However, all the decomposition temperatures were significantly higher than the upper reflow temperatures of lead-free profiles. It should also be noted that whilst the measured values varied by 20°C, the quoted values had a larger (x2) variation i.e. 40°C.

Table 11: Comparison of measured Td values and the typical values quoted by the laminate supplier

Material	Decomposition temperature	Typical suppliers' quoted value
SD	295°C	320°C
SP	310°C	350°C
HD	295°C	310°C
HP	315°C	350°C

4.4 PERIODIC MONITORING THERMAL CYCLING

For periodic electrical resistance monitoring the failures were mainly restricted to the standard Tg dicy-cured material. This material gave a significantly lower performance than alternative materials tested because, as detailed previously, it suffered from a high CTE both above and below the glass transition temperature, as well as a low Tg. Results for 10:1 vias in boards of this material are presented in Figure 30. Clearly boards processed at the higher reflow temperatures had a significantly higher failure rate, with a possible “step function” associated with raising the reflow peak temperature above 245°C. This is illustrated by the better performance of boards subjected to 6 passes at 245°C compared to those conditioned for 3 profiles at 260°C. The trends in improving fatigue life by reducing the number of reflow passes or by reducing the peak reflow temperatures, are clearly indicated for the SD material.

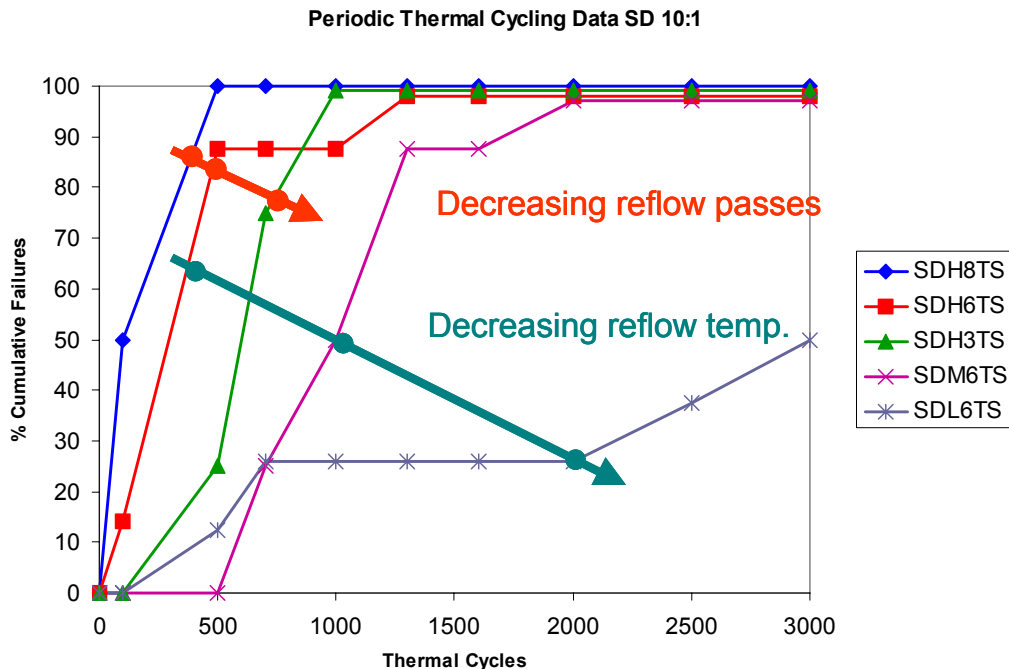


Figure 30: Comparison of cumulative periodic monitoring electrical test failures during thermal cycling for 10:1 vias in SD material with three conditioning profiles (230, 245 & 260°C), and for 3, 6 and 8 reflows

Figure 31 demonstrates similar results for the 8:1 vias with the SD material. Again, boards processed at the higher reflow temperatures had significantly higher failure

rates associated with raising the reflow peak temperature above 245°C. Again, boards subjected to 6 passes at 245°C performed significantly better compared to those conditioned for 3 profiles at 260°C. Similar trends in improving fatigue life by reducing the number of reflow passes or by reducing the peak reflow temperatures, are again clearly indicated.

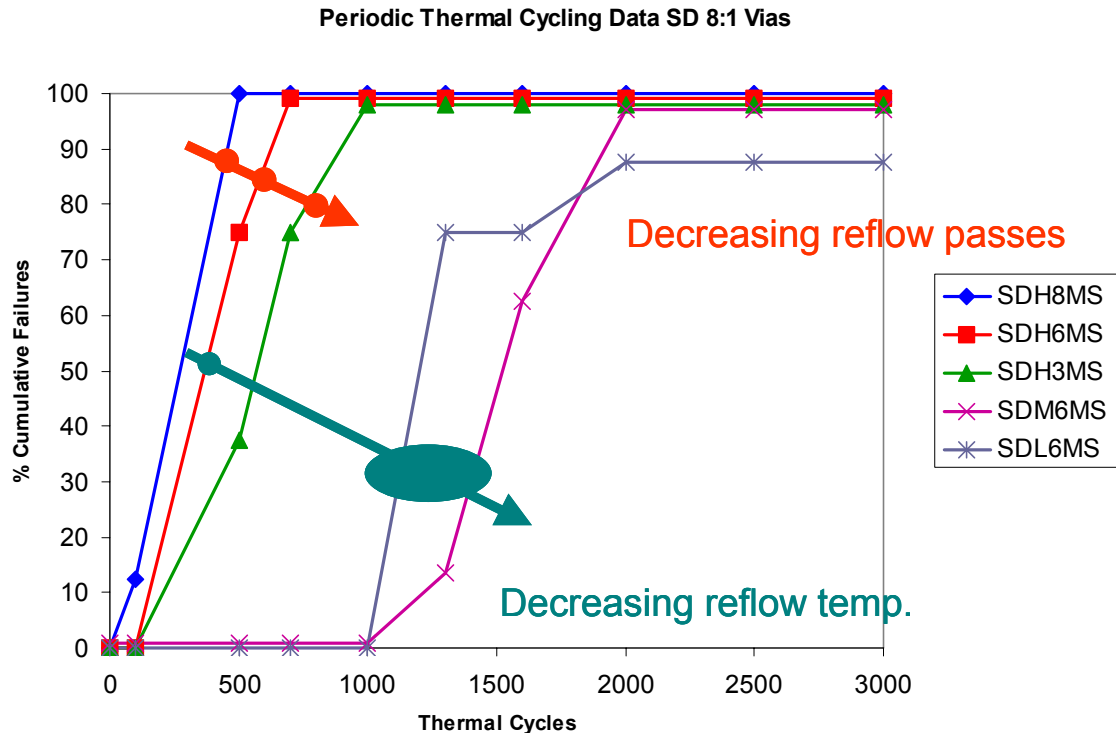


Figure 31: Comparison of cumulative periodic monitoring electrical test failures during thermal cycling for 8:1 vias in SD material with three conditioning profiles (230, 245 & 260°C), and for 3, 6 and 8 Reflows

A comparison of the cumulative failures for 10:1 vias thermally cycled after 6 reflows at 260 °C in all four board materials, is provided in Figure 32. The two materials exhibiting the worst performance were SD and HD, the materials with the highest CTE above and below their glass transition temperatures. The HD material has the higher T_g, and therefore slightly improved performance over the SD material.

Figures 33 to 36 present images of typical 10:1 vias after thermal cycling. In all sections, concertina-like collapsing of the vias was present, with fatigue cracks in all copper barrels. Failures were generally through the centre of the via barrel. However, with the HP and SP materials, the concertina-like collapsing was less heavy and the nickel outer plating on these vias was not ruptured, maintaining the electrical continuity of the via. If these boards had been finished without the nickel plate (as in the case of OSP or silver finish), these boards would have exhibited significantly more failures.

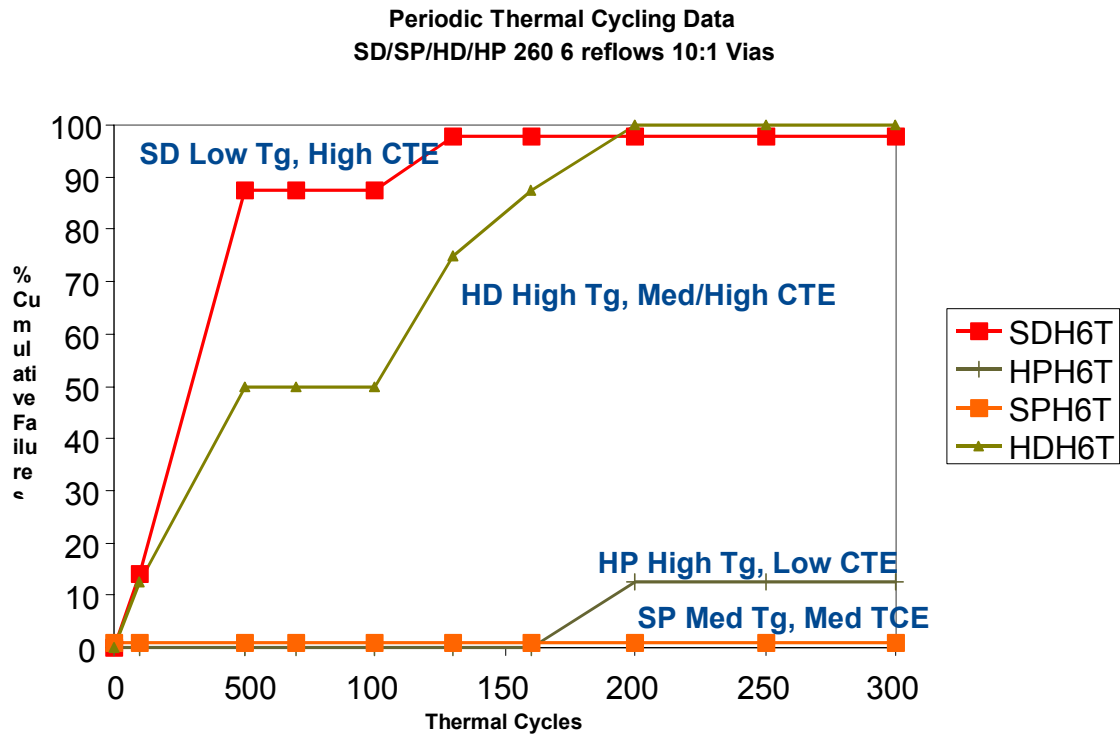


Figure 32: Comparison of cumulative periodic electrical test failures during thermal cycling for 10:1 vias, for four material types (SD, SP, HD & HP), for 6 reflows and a peak reflow temperature of 260°C

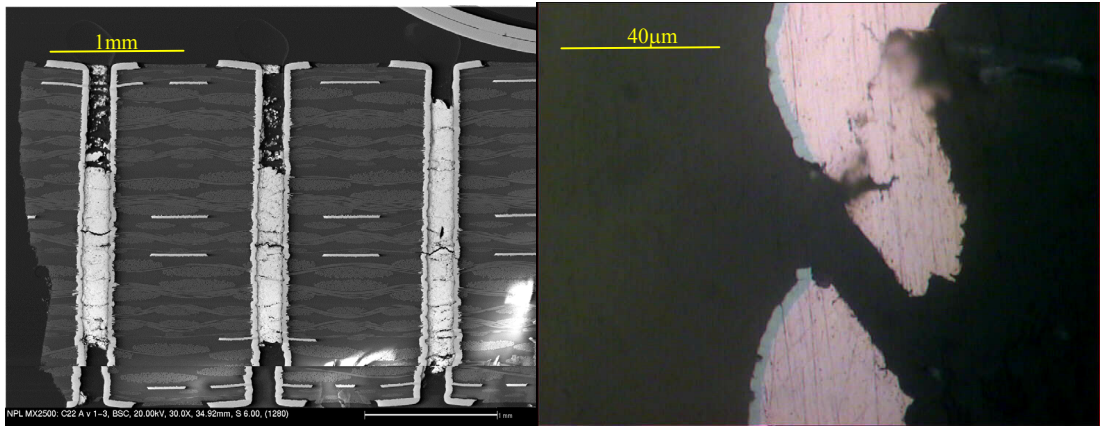


Figure 33: Micro-sections of typical 10:1 via in SD material after 2000 thermal cycles showing heavy concertina-like collapsing of vias, and failure of copper and nickel in the via wall

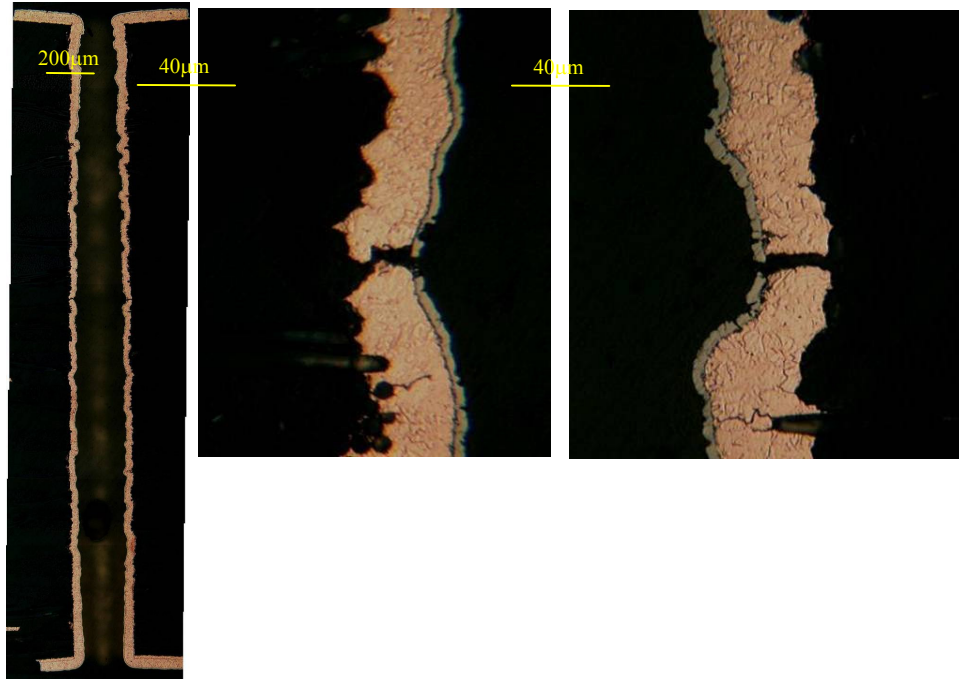


Figure 34: Micro-sections of typical 10:1 via in HD material after 2000 thermal cycles showing heavy concertina-like collapsing of vias, and failure of copper and nickel in the via wall

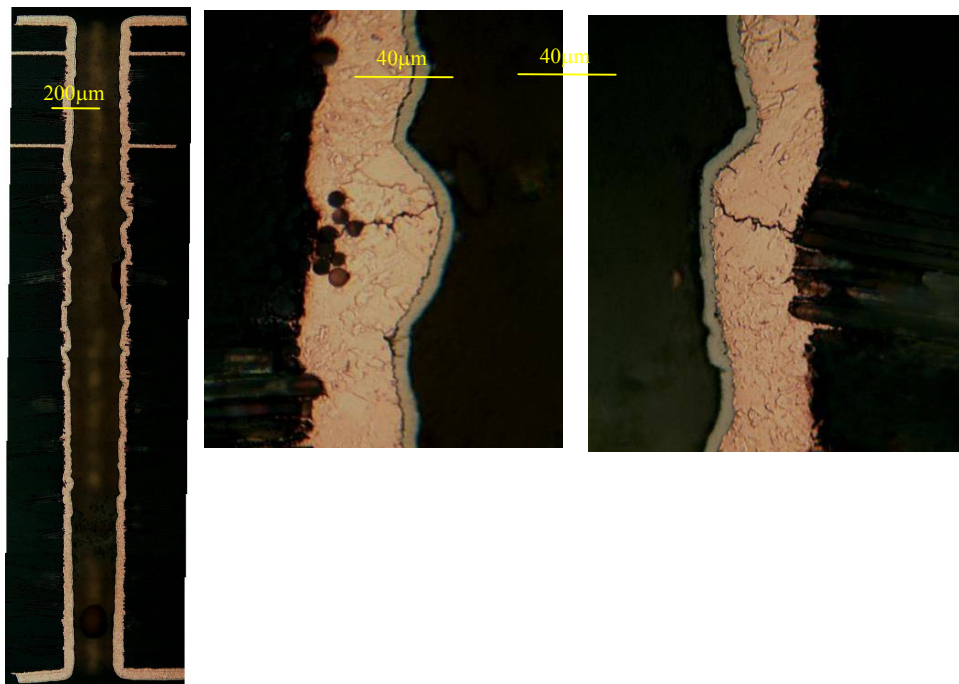


Figure 35: Micro-sections of typical 10:1 via in SP material after 2000 thermal cycles showing heavy concertina-like collapsing of vias, and failure of copper but intact nickel at the via wall

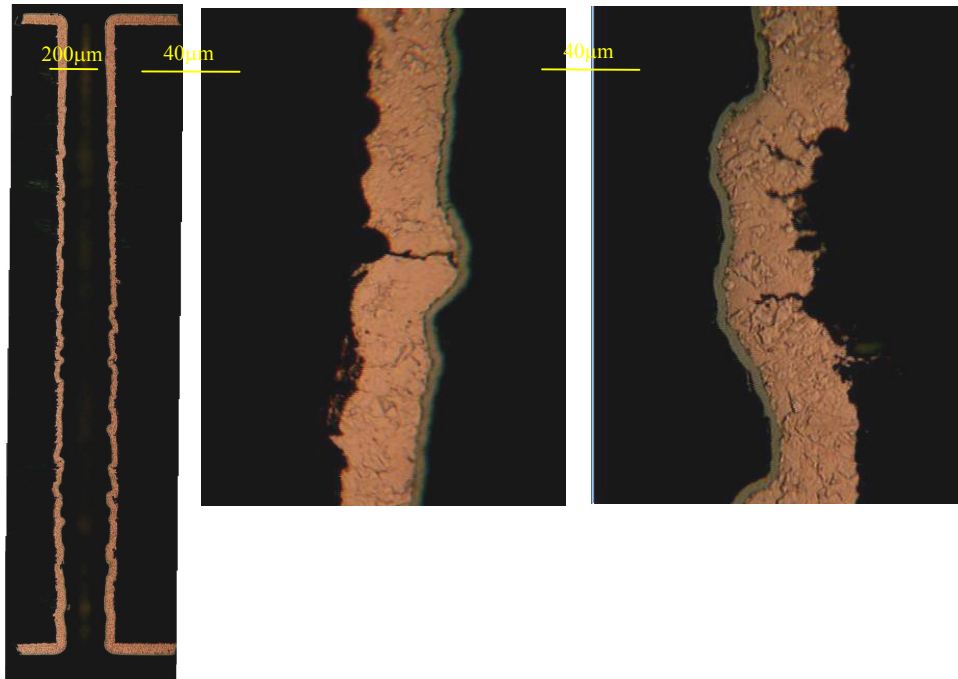


Figure 36: Micro-sections of typical 10:1 via in HP material after 2000 thermal cycles showing concertina-like collapsing of vias, and failure of copper but intact nickel in the via wall

Figure 37 provides a comparison of the cumulative failures for 8:1 vias thermally cycled after 6 reflows at 260°C on all four board materials. Comparing these data with those of the 10:1 failures, there is little difference for the SD material. Its high CTE again produced increased stress on the vias and earlier failures. However, for these larger aspect vias, the HD material exhibited much improved fatigue life performance. As with the 10:1 results, there were few failures for the SP material. However, for the HP material, there were increased failures compared with the 10:1 via data.

The probable cause for these premature failures is highlighted in Figure 38. The nickel layer, which was intact for the 10:1 HP vias in

Figure 36, had been fractured for the equivalent 8:1 via shown on the right in Figure 38. It should be noted that compared to the thickness of the nickel of the SP material shown in the left of Figure 38, that for the HP material was significantly less, resulting in the earlier failure i.e fewer thermal cycling failures. The 10:1 vias did not contain the thinner nickel layer. Again, in the SP material, fracturing of the copper barrel was evident, but the nickel barrier was intact, maintaining the electrical continuity of the vias.

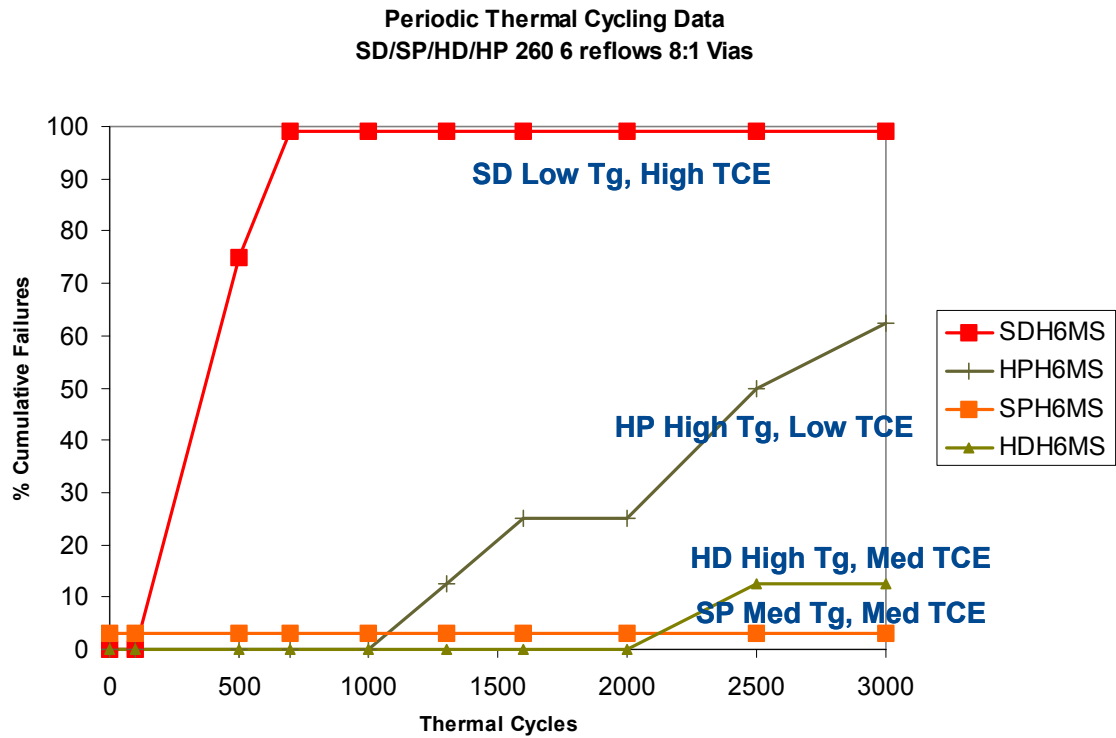


Figure 37: Comparison of cumulative periodic electrical test failures during thermal cycling for 8:1 vias, for four material types (SD, SP, HD & HP), for 6 reflows and a peak reflow temperature of 260°C

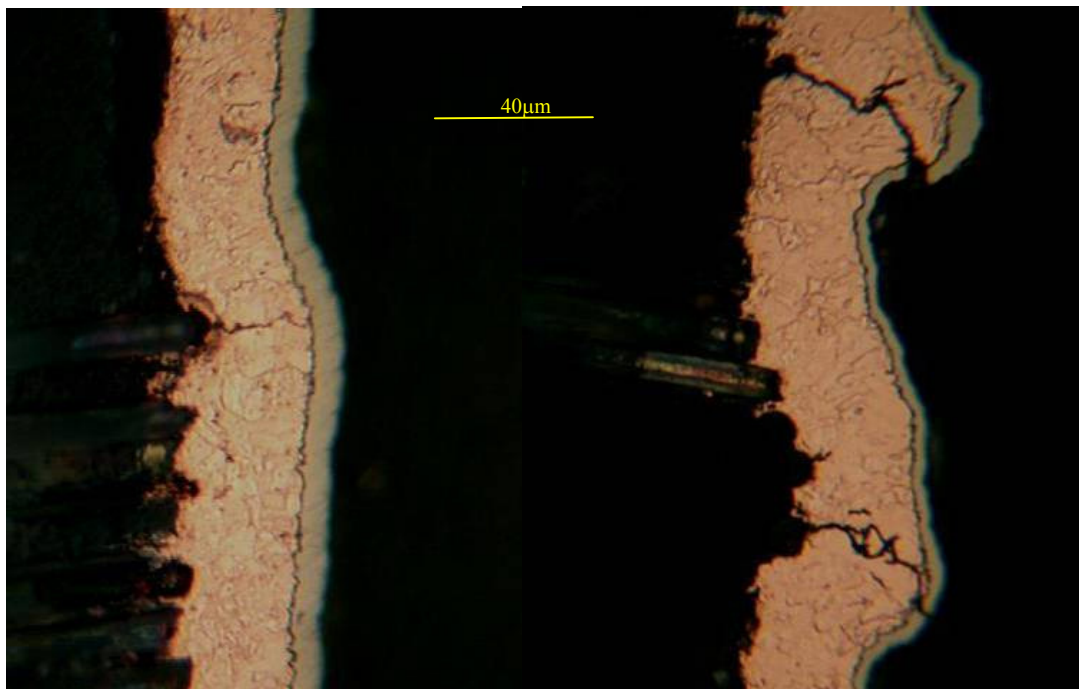


Figure 38: Comparison of micro-sections for SP (left) and HP (right) showing differences in nickel thickness on 8:1 via walls

For 6:1 vias and micro-vias, the only significant failures occurred in the SD material (Figure 21 and 22). In both cases, more failures occurred with higher processing temperatures and with a greater number of reflow profiles. The annotated data for the 6:1 via data are shown in Figure 39. Indeed, for the micro-vias, significant failures only occurred for six and eight reflows at the 260°C peak temperature profile.

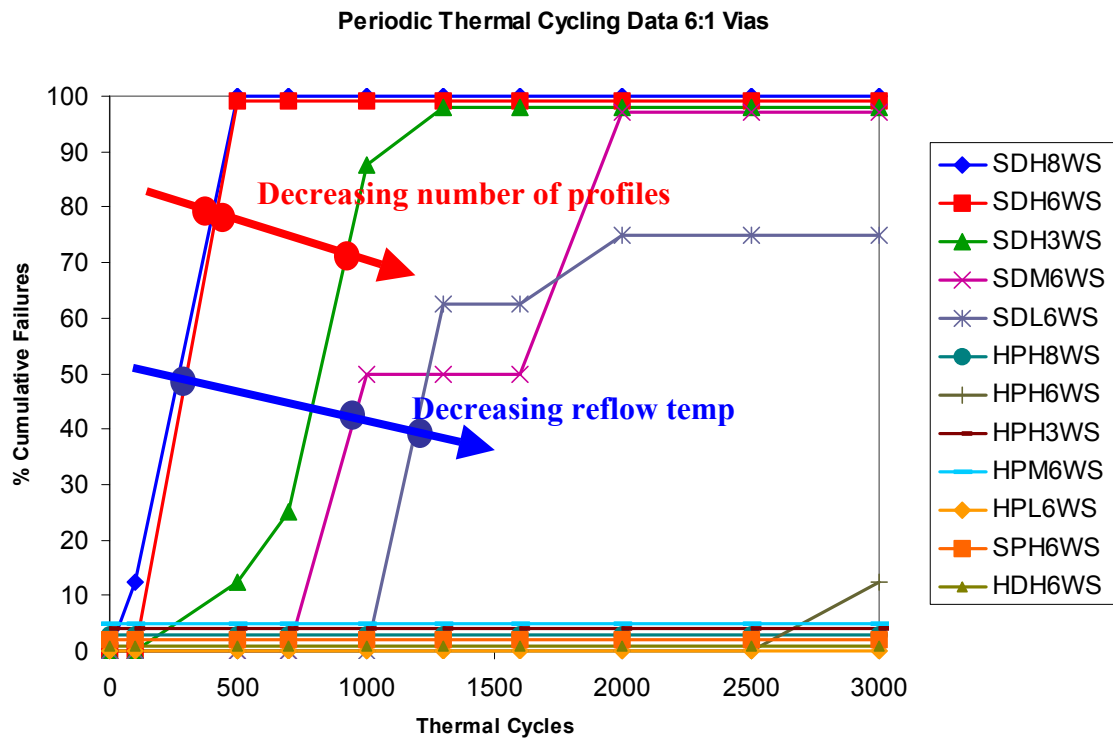


Figure 39: Annotated cumulative periodic electrical test failures during thermal cycling for 6:1 vias, for four material types (SD, SP, HD & HP), three conditioning profiles (230, 245 & 260°C) and for 3, 6 and 8 reflows

4.5 CONTINUITY MONITORING DATA

For those samples continuously monitored, failures were restricted to the larger aspect ratio samples. There were no failures in the 6:1 vias for the SP, HD or HP materials for 6 reflows at 260°C. Moreover, the SP material did not exhibit any failures for 8:1 vias. Continuous monitoring was not undertaken on micro-via samples..

The annotated data shown in Figures 23 to 27 exhibited similar trends to those of the periodically monitored data - decreasing via aspect ratio or decreasing peak reflow temperature, resulted in increased cycles to failure. The poorer performance of the SD material can again be attributed to its high CTE and low T_g. There were few differences in the trends in performance between samples having different aspect ratios for the SD material reflowed at 260°C peak reflow temperature.

Table 12 and again display the trends highlighted after periodic monitoring; the SD material performs poorer than the HD, SP and HP materials, the higher aspect ratio samples perform better, as do samples subjected to lower peak reflow temperatures.

Table 12: Calculated $N_{(1\%)}$ failure values

Material	Reflow °C	Passes	10:1	8:1	6:1
SD	230	6	550	450	1000
SD	260	6	60	100*	45
SP	260	6	700	-	-
HD	260	6	150	450	-
HP	260	6	500	1000	-

A comparison between periodic monitoring data and continuity monitoring data for the same data sets, is presented in Figure 40. In the case of periodic monitoring, the failures clearly develop at a later stage even though the failure criterion ($>100\Omega$) is less than that for the continuous monitoring ($>3K\Omega$). The first failure with the periodic monitoring occurs at approximately double the number of cycles observed in the continuous monitoring. The via failures initially develop as intermittent contacts (captured by the continuous monitoring), and are generally observed above 60°C on the positive ramp. When the vias have cooled to room temperature (where periodic monitoring is undertaken), the vias have contracted, and the small fatigue cracks have closed, thus reviving the continuity through the via.

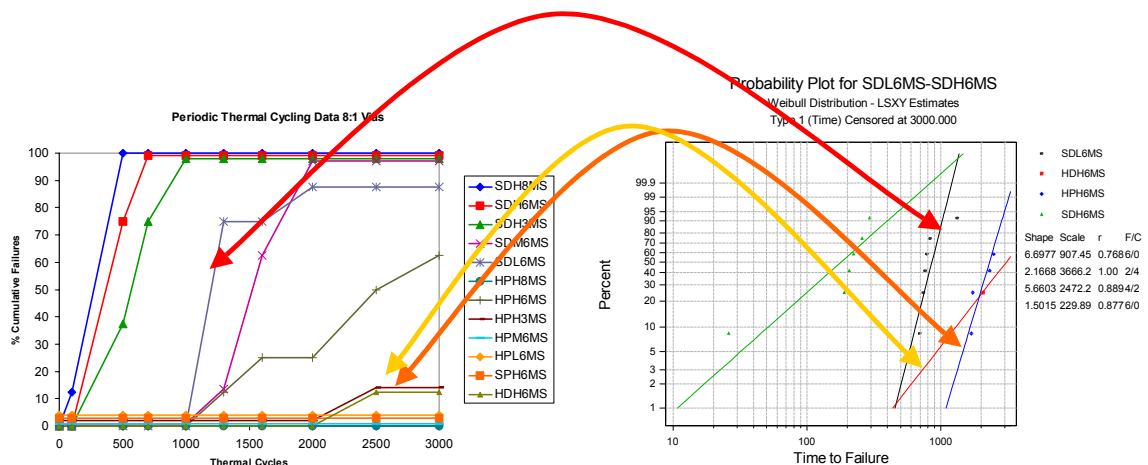


Figure 40: Comparison of periodic monitoring data and continuous monitoring data

5 CONCLUSIONS

PCBs have been fabricated using four different base laminate materials commonly used by the electronic industry. These materials were both standard and high glass transition temperature (T_g) epoxy systems, with both dicy and phenolic curing agents. The assemblies were conditioned using reflow soldering profiles with peak soldering temperatures of 230, 245 and 260°C, for up to 8 reflows. After conditioning, the assemblies were thermally cycled for up to 3000 cycles and the electrical resistance of 10:1, 8:1, 6:1 and micro-vias was monitored.

The fatigue failures generated by thermal cycling were dominated by barrel cracking. Micro-sectioning of failed vias showed heavy concertina-like collapsing of barrels, and fatigue cracks through the copper walls. In the vias where the stress during reflow was highest (i.e. materials with a high z-axis CTE, high aspect ratio vias, and/or higher number of reflow profiles), the nickel over-plate was also fractured causing via failure. In other cases, copper failures were still present but the nickel was intact. These thermal cycling failures generally occurred at the mid-point through the board, within the barrel.

For the standard T_g dicy-cured material, the majority of via chains conditioned with a peak reflow temperature of 260°C, had failed by 1000 thermal cycles, irrespective of via aspect ratio. Lowering the peak reflow temperature to 245°C extended the fatigue life to around 2000 cycles. When the reflow temperatures were further lowered to SnPb processing levels (230°C peak) then some SD via chains remained intact after 3000 cycles. For the other materials, the majority of via chains survived 3000 thermal cycles, even for 10:1 aspect ratio vias. The exception was the 10:1 vias in the HD (high T_g dicy-cured) material. Although this material had a high T_g, its z-axis CTE was higher than that of the SP (standard T_g phenolic-cured) or HP (high T_g phenolic-cured) materials, and this resulted in earlier failures. Significant failures were also noted for the HP material for 8:1 vias conditioned with a 260°C peak reflow temperature. Micro-sections of failed joints highlighted thinner nickel plating on these vias, which may have contributed to their earlier failure.

Comparison between the batches of PCBs allowed the following conclusions:

- Higher processing temperatures result in earlier failures
- Increasing peak reflow temperature above 245°C may significantly increase the failure rate, and may result in a “step function” decrease in lead-free reliability
- Increasing the number of profiles results in earlier failures
- Higher aspect ratio vias fail earlier than lower aspect ratio vias
- Materials with high z-axis CTE performed worst during thermal cycling
- Increasing T_g improves via reliability, but lower T_g, lower CTE materials have been shown to out perform higher T_g, higher CTE materials

Some samples were monitored for electrical resistance both periodically (every 500 cycles) or continuously. In the case of periodic monitoring, the failures clearly developed at a later stage even though the failure criterion (>100Ω) was greater than

that for the continuous monitoring ($>3K\Omega$). In the case of continuous monitoring typically failures initiate at 50% to 75% of the fatigue life for the first failures for periodic monitoring. The failures first develop as intermittent contacts which are measurable as short duration open circuits, generally on the positive ramp, approximately at 80°C. By the time the vias have cooled to room temperature (where the periodic monitoring measurements are undertaken), the vias have contracted, closing the small fatigue cracks and reviving the continuity through the via.

The first phase of this work has shown that a test method for testing these materials is achievable. The test is sensitive for measuring the effect of the higher temperatures associated with lead-free soldering on the reliability of electronic substrates. The results from these tests will improve industry confidence in the reliability of PCB substrates during and after the change to lead-free processes.

6 ACKNOWLEDGEMENTS

The work was carried out as part of a project in the Materials Processing Metrology Programme of the UK Department for Innovation, Universities and Skills. We gratefully acknowledge the support and co-operation of the following companies without whose help this project would not have been possible.

BAE (INSYTE)
Circatex Limited
Dolby Laboratories Inc. (UK)
Fujitsu Telecommunications Europe Ltd
Goodrich Engine Controls
Graphic Plc
Isola Werke UK Limited
MBDA (UK) Ltd
NEC
Panda Europe
Polar Instruments UK Ltd
Polyclad Europe
PWB Interconnect Solutions Inc
Rockwell Collins
Rolls Royce Marine
Substrate Systems Limited (SSL)
Thales Missile Electronics Ltd
TRW Automotive Technical Centre, Solihull

In addition, we would like to acknowledge the material support provided by the following individuals and companies, which made the project possible.

Gerald Rutter and Peter Franklin, BTU Europe
Paul Comer and Kerry Hewlett, Graphic Plc
Sam Gnaniah, Roger Morrell, Madeleine Peck and Ling Zou, National Physical Laboratory
Bill Birch and Jason Furlong, PWB Interconnect Solutions Inc
Dave Hillman and Bob Miller, Rockwell Collins for some of the sectioning
Mark Newton and Mick White, Thales Missile Electronics Ltd

7 REFERENCES

- (1) PWB Corp. IST report, private communication
- (2) *Glass transition temperature of organic films - DMA Method*
IPC-TM-650 2.4.24.2
- (3) *Thermal analysis techniques for composites and adhesives*
D R Mulligan, S J P Gnaniah, G D Sims,
NPL Good Practice Guide GPG 62. 2002
- (4) *Standard test method for rapid thermal degradation of solid electrical insulating materials by thermogravimetric method (TGA).*
D3850-94. 2006