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**Test Method for Conformal
Coating Protection
Performance of Electronic
Assembly in Harsh
Environments**

Ling Zou and Chris Hunt

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Test Method for Conformal Coating Protection Performance of Electronic Assembly in Harsh Environments

L Zou and C Hunt
Engineering and Process Control Division

ABSTRACT

This report describes new developments for a test method for assessing conformal coating protection performance on electronic assemblies using the Surface Insulation Resistance (SIR) technique. The new method is significantly different to the existing standard¹ in a number respects and reflects more realistic application of conformal coatings. A new test assembly is introduced with a wide range of components, and has many advantages in identifying coating protection problems. The procedure on how to chose and apply contaminants to test coupons to simulate the contaminants effect from harsh environments on underlying circuit reliability is detailed in the method. The test parameter settings for SIR test and SO₂ exposure testing are given. The test method provides a measurement tool to discriminate between coatings.

The use of this method to investigate the protection performance of seven different types of coatings (two water-based acrylics, solvent-based acrylic, fluoroacrylate, silicone, polyurethane, and epoxy) against solvent-based flux, surfactant and SO₂ gas, is included in an appendix. These results demonstrate that SIR technique is a suitable discriminatory tool for coating performance assessed, and is sensitive in detecting the circuit reliability underneath coatings. Coating type affects the level of protection against specific contaminants i.e. coatings are contaminant-sensitive. Coating protection performance is not only dependent on coating and contaminant type, but also the component type where shape factor and coating coverage is an issue. Therefore, the results on protection performance of conformal coating using this new test method and test board design provides more realistic and useful information on the protection performance of conformal coating against specific harsh environment in which electronic circuits operate.

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1 INTRODUCTION

Achieving high reliability in service is the key issue in today's electronics manufacture. Electronics are now being used in a wide range of applications and under increasingly severe conditions, and the challenge is to maintain higher levels of reliability in these hostile environments, particularly in safety critical applications.

Contaminants, either from manufacturing processes or the environment, can cause leakage currents; which degrade circuit functionality. When ionic and hydrophilic contaminants reach the circuit board surface (under the coating and with the metal conductors), leakage currents will occur. Furthermore if the contaminants are corrosive and mobile, they can migrate and react with the metals on the circuit board to generate conductive products. These corrosion products may then in turn migrate and further degrade the circuit operation. Catastrophic failure occurs when the corrosion products form a dendrite-like growth of metallic compounds, causing a short circuit between adjacent electrodes. Besides a short-circuit failure, an open circuit failure may also result when there is extensive localised corrosion along a thin conduction line.

Conformal coatings have been applied for electronic circuits to achieve a high degree of protection, even in environments that would normally be considered hostile for electronic equipment^{1,2}. Conformal coatings are a compromise from full enclosure, such as potting, since element of access, or rework, are designed at a later date. Hence coating should be robust and protect the surface, but can be removed if necessary for repair of component. Coatings are typically semi-permeable membranes and can prevent contaminants instantaneously reaching the circuit, but will not be completely impermeable to the wide range of contaminants. Previous work has demonstrated that permeation of contaminants is dependent on coating material (molecular chemistry), coating coverage, contaminant and concentration of contaminant^{3,4}. However, there is no standard test method to evaluate the extent and nature of the protection coating afforded against a specific aggressive environment. Existing test method¹ determine the insulation resistance of on a bare PCB with an applied conformal coating under prescribed conditions of temperature and humidity, but no contaminants are involved to represent harsh environments. A test method based on a simple bare PCB test coupon will not represent real electronic assemblies, as the issue of coating coverage around components are not assessed. Work previously showed that coating coverage plays an important role on coating protection performance, with failure developing at the weakest point of the coating³. Therefore a test method needs to be developed and updated that address these issues.

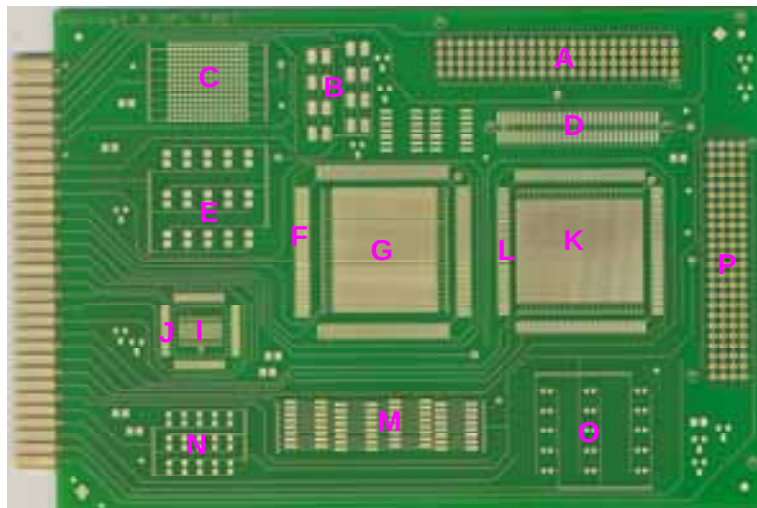
A method is described here that assesses coating protection performance from aggressive environments, and that has been validated using seven different coating types against three selected contaminants that reflect some harsh environments for electronic circuit. These contaminants were selected from earlier studies and are considered representative of generic types that are most harmful of the mostly uncounted types

2 TEST METHOD

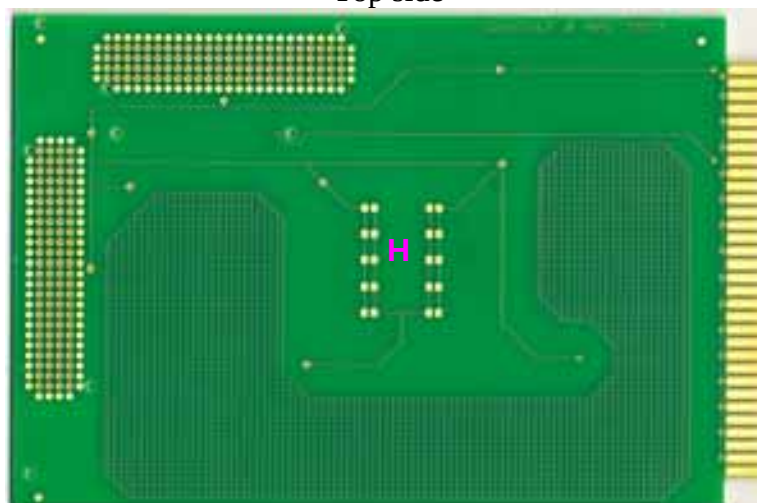
2.1 EQUIPMENTS AND MATERIALS

2.1.1 Test board

A specially designed test board is shown in Figure 1, and shows component pad positions and associated surface insulation resistance (SIR) patterns. The coupon should be manufactured from epoxy FR-4 laminate with 17 μ m(1/2 oz) thick copper track with a AuNi finish and has solder mask. The board is assembled using 13 component types as shown in Figure 2. The component details and suppliers are listed in Table 1. The components should be dummy insulated components have high resistance ($\geq 10^{11}\Omega$). Sixteen SIR test patterns, A-P, are incorporated into the design. There are 9 types of surface mount components and two types of wave reflow components on the assemblies. The assembly process and solder materials should be the same as the manufacturing process being evaluated.



Top side

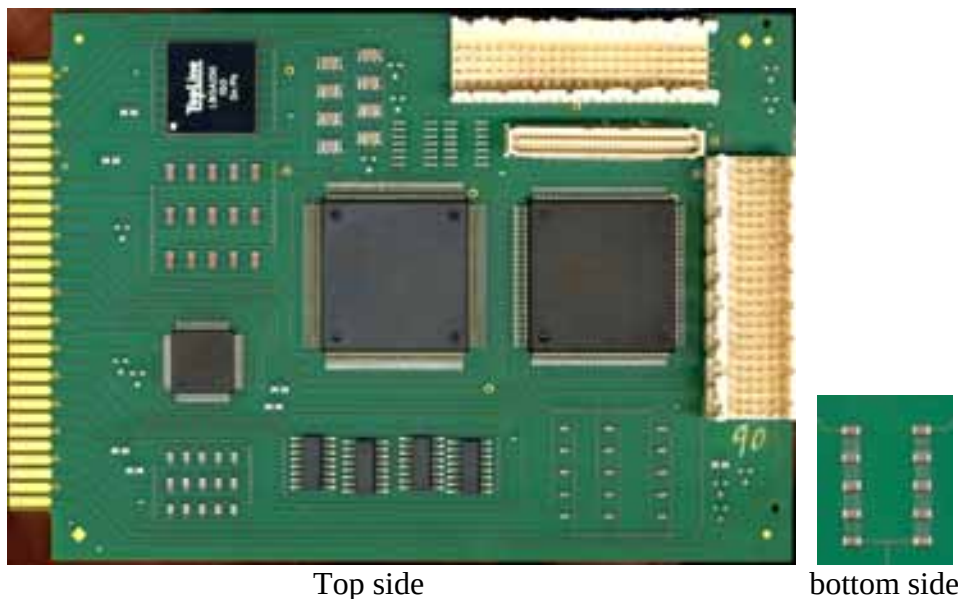


Top side

Figure 1. Layout of test board NPL TB57

Table 1: Dummy component details

ID	Component	SIR Gap [mm]	Manufacture Type
A	TH connector 4x24 pins horizontal	0.6	24x4=96 way AMP: 536501-3
B	8 x SM Cap 1210	0.6	Practical Components:1210SMC-PL
C	BGA256, 1mm pitch	0.4	Topline:BGA256T1.0-ISO
D	SM connector IEEE 1386, 2 x 16 pins	1.0	Molex:1.00mm (.039") Mezzanine IEEE 1386 SMT, Dual Row, 71436
E	15 x SM Cap 0805	0.6	Practical Components 0805SMC-PA
F	QFP160 0.65mm pitch ISO	0.254	Practical Components: QFP160-28mm-.65mm-2.6 (isolated)
G	COMB under QFP160	0.2	
H	10 x SM Cap 0805	0.6	Practical Components: 0805SMC-PA
I	COMB under QFP80	0.2	Topline: A-TQFP80-12mm-.5mm-2.0 (Amkor)
J	QFP80 0.5mm pitch ISO	0.2	'Practical Components: QFP128-28mm-.8mm-2.6 (isolated)
K	COMB under QFP128	0.2	
L	QFP128 0.8mm pitch ISO	0.3	Practical Components: QFP128-28mm-.8mm-2.6 (isolated)
M	4 x SOIC16 1.27mm pitch ISO	0.2	Practical Components: SO16GT-3.8mm
N	15 x SM Cap 0603	0.6	Practical Components: 0603SMC-PA
O	15 x SM Cap 0402	0.6	Practical Components: 0402SMC-PA
P	TH connector 4x24 pins vertical	0.6	24x4=96 way AMP: 536501-3



Top side

bottom side

Figure 2. Test assembly

2.1.2 Humidity chamber

A chamber capable of achieving temperature and humidity environments of up to $90 \pm 0.2^\circ\text{C}$, and $93 \pm 5\%$ relative humidity (RH). The chamber should be constructed with stainless steel inner surfaces and be well insulated. The temperature and humidity measurements should be taken using sensors such as dry and wet bulb thermometers. Solid state sensors cannot tolerate high temperature and humidity. The temperature humidity levels of the test chamber shall be recorded throughout the test, preferably with independent control sensors.

2.1.3 High resistance measurement system

The measurement system shall comprise

- A measuring device capable of measuring surface insulation resistance (SIR) in the range of 10^6 ohms to 10^{12} ohms.
- A test and bias voltage supply capable of providing 5 and 50 volts DC ($\pm 2\%$).
- A sample selection system capable of individually selecting all the test patterns in the measurement experiment. The system shall incorporate an in-line limiting resistor of 10^6 ohm or greater in each current pathway. The tolerance of the total measurement system shall be $\pm 5\%$ up to 10^{10} ohms, $\pm 10\%$ between 10^{10} to 10^{11} ohms, and $\pm 20\%$ above 10^{11} ohms. A calibration board is required to run this calibration check, as shown in Figure 3.
- The data sampling rate should be every ten minutes.

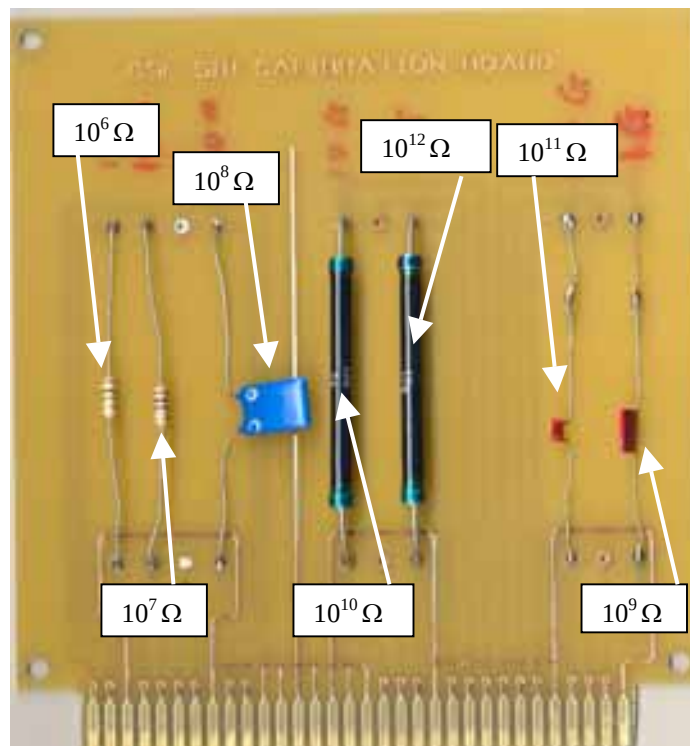


Figure 3. The calibration board

2.1.4 Test board holders

The test board holder is an arrangement of equally spaced (minimum of 15 mm spacing) 32-way gold edge connectors 0.1 in. pitch single sided mounted on a stainless steel frame. The cabling from the test holder to the outside of the humidity chamber should be accomplished using Halogen-free 0.05 in. pitch cable with 34 conductors. The cleanliness of the test board holder, the connector block and the cables should be assured. Cleaning with a contamination meter is ideal, but other approaches are acceptable. After cleaning the equipment should be tested without a board plugged in, and then the resistance should be checked with the calibration board.

2.1.5 Contaminants

The reliability of circuitry is of great concern, especially when operated under severe environmental conditions, e.g. marine environments, industrial gas pollution (SO₂, NO₂, HCl), surfactants, hydraulic fluids and de-icing fluids. For accelerated testing, selecting a suitable chemical at the correct concentration to represent these environmental condition is very important, and should represent where circuits are going to be exposed. The chemicals can be dissolved in either distilled water or isopropyl alcohol. In a previous report some chemicals have been successfully selected to represent several environment conditions⁴.

2.2 COATING APPLICATION

The coatings can be applied by the preferred industry process, this will typically include both dipping and spraying in accordance with coating supplier recommended standard procedures. The edge connector on the test assembly needs to be masked, and must not receive any coating.

2.3 TEST BOARD CONTAMINATION

2.3.1 Contaminant solution

For the contaminant solution a certain volume and contamination area for each test pattern need to be defined, as shown in Figure 4, to ensure the same contaminants concentration on each type component. The defined volume of contaminant solution is slowly applied into the defined yellow line areas for each test pattern as a number of drops using, initially onto the centre of the area, and then to ensure a uniform coverage, by dispensing further drops in areas of low coverage. The test vehicle is held horizontally through out the contaminant application and drying period. The aim is to achieve a uniform thickness of the contaminant over the SIR pattern, and to avoid the contamination spreading outside the pattern. However some conformal coatings have high surface energy, and some contaminants will not wet very well, so smaller drops of the contaminants are dispersed widely across the whole of each pattern. Contaminated assemblies shall be left to air dry for up to two hours before SIR testing.

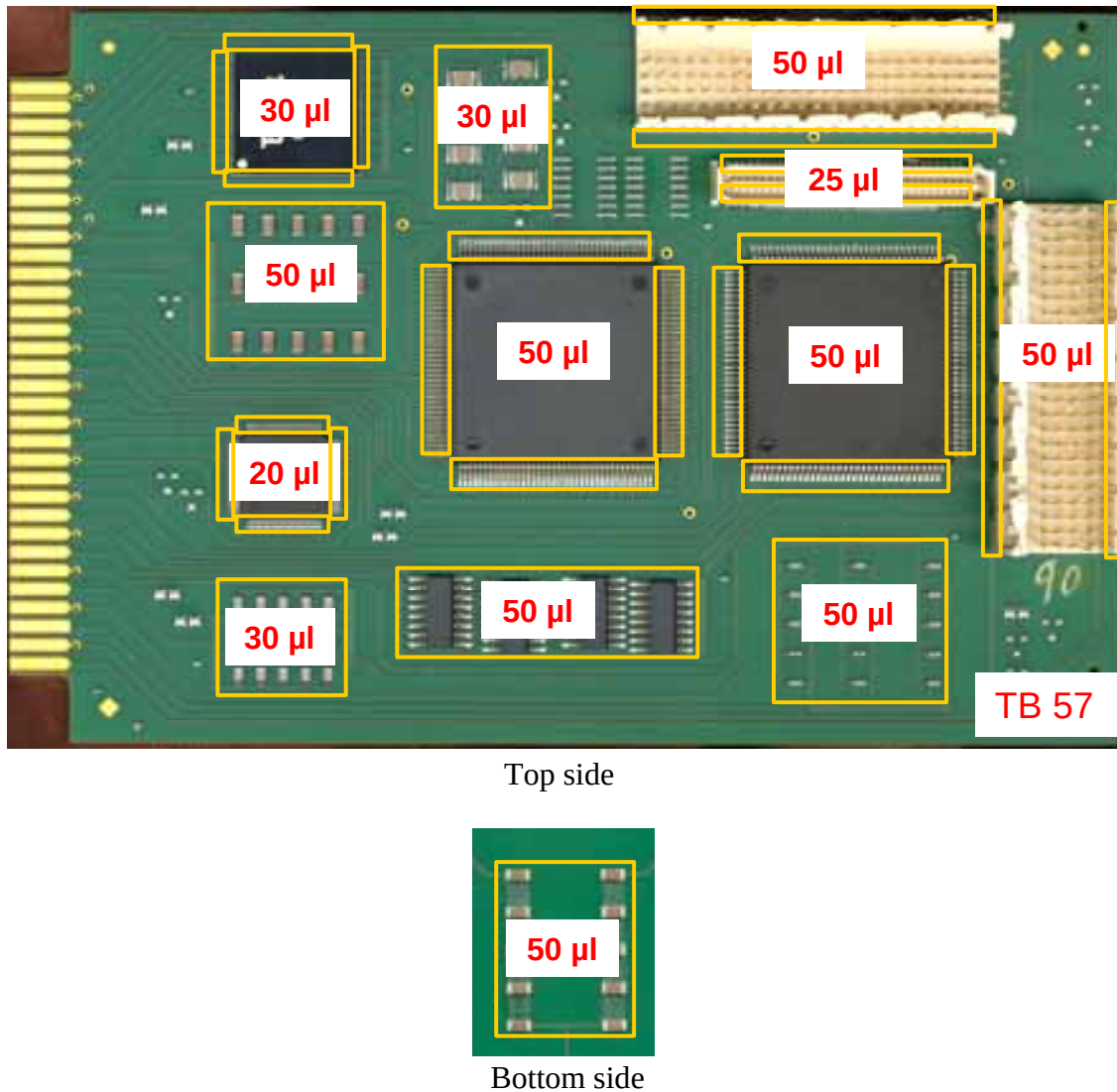


Figure 4. Contaminant volume and contamination area for each test pattern

2.3.2 Industry gas pollution

For exposure to polluting gases, the exposure time, temperature, humidity and concentration of the polluting gas shall be defined according to application or relevant standard. For SO₂ exposure, the following conditions are suggested for best discrimination between different coatings, 0.33% SO₂ at 23°C for 96 hours. Following exposure assembly should be SIR tested as soon as possible, normally less than 2 hours.

2.4 SURFACE INSULATION RESISTANCE MEASUREMENTS

2.4.1 Sample size

At least three test assemblies for each coating shall be SIR tested.

2.4.2 Test parameters

Two sets of test parameters are recommended. Test conditions of 40°C/93% RH with 5V should be used for contaminated boards, and 40°C/93% RH with 50V bias should be used to increase equipment sensitivity, when qualifying bare boards.

2.4.3 Test assembly measurement.

Carefully mount the test boards, in the vertical plane in the humidity chamber, and connect the wiring loom from the boards to the outside of the measuring chamber. Subsequently bias can be applied. SIR measurement should be started first before ramping up temperature and humidity.

The high resistance measurement system is used to monitor the SIR values. SIR measurements shall be performed under constant temperature and humidity conditions. The temperature shall be ramped up first and allowed to equilibrate, before the humidity is increased. The humidity shall be increased slowly enough to avoid condensation on the board. A DC bias voltage shall be continuously applied across the comb patterns during the test period of 72 hours, and the SIR measured every 20 minutes. The instrument shall include a $10^6 \Omega$ resistor on each test channel to preserve any dendrites that form, hence the minimum SIR measurement value of the system is $10^6 \Omega$.

The coated assemblies shall be tested without any contaminant for 24 hours, the results can be used for a benchmark.

2.5 TEST REPORT

The test report shall include the following information:

- a) Coating name and type.
- b) Chemical species and concentration of applied contaminants, and volume applied for each test pattern.
- c) Test conditions; temperature, humidity and bias voltage for uncontaminated assembly and contaminated assembly.
- d) The individual graphs showing the average log SIR value on repeated boards with time for each test pattern and test assembly.
- e) If any SIR results show a rapid change in resistance of one order of magnitude in less than one hour, then these occurrences should be examined under a microscope with back-light to check for the presence of dendrites and corrosion product formation. However, for this test assembly dendrite and corrosion products may not be easily inspected as they may be covered by components, and these shall be removed if it is necessary. Any dendrite, corrosion product and discolouration during the SIR test shall be recorded in the report

- f) Brief explanation and conclusion of test results.

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APPENDIX A: TEST METHOD VALIDATION

A.1 TEST ASSEMBLY

Forty-five TB57 PCBs with a solder mask, and insulated dummy components were supplied to two assembly manufactures, A and B, to build test assembly in accordance with their own production process. They both used no-cleaning SnPb soldering process.

A.2 COATING MATERIAL

Seven different coating chemistries from six coating suppliers were used (two different water-based acrylics, solvent-based acrylic, silicone, polyurethane, fluoroacrylate and epoxy). Four TB 57 assemblies from each assembly manufacturer were coated by each of the material suppliers, in accordance with their own recommended standard procedures, one TB67 PCB was also coated. The coatings were applied by dipping, except for the water-based acrylic (1) coating, which was applied by both dipping and spraying. Two coatings, the water-based acrylic (2) and the silicone, were double dipped to investigate the effect of the coating thickness on protection performance. The details of the test boards with their coatings are listed in Table A.1.

Table A.1 Test assembly

Test assembly	Appl. method	Coating
4 TB57 A assembly 4 TB57 B assembly 1 TB67 PCB	Single Dip	Water-based acrylic (1)
		Water-based acrylic (2)
		Solvent-based acrylic
		Silicone
		Polyurethane
		Epoxy
		Fluoroacrylate
	Spray	Water-based acrylic (1)
	Double Dip	Water-based acrylic (2)
		Silicone

A.3 CONTAMINANTS

Three contaminants were selected to evaluate coatings, a solvent based commercial flux, a common surfactant and SO₂ gas. The details for these three contaminants are listed in Table A.2.

Table A.2. Contaminants detail

Contaminant	Concentration (by weight)	Main constituents
Commercial flux	15% in IPA	Adipic, Succinic and Glutaric Acid
Amphoteric Surfactant	1% in DI water	Lauryl Betaine
Pollution Gas	0.33% in air	SO ₂

A.4 TEST BOARD CONTAMINATION

For two contaminants, flux and surfactant, the test boards were contaminated according to the test procedure in 2.2. However, the test assemblies were not fully assembled by all partners due to late delivery of some components. The contamination area and contaminant volume were slightly different from that in section 2.2, and details are shown in Figure A.1. Each contaminant was applied to each of the coating types. So from each assembler there were 2 boards with the same contaminant and coating.

For the SO₂ gas, a single TB67 PCB for each coating was exposed in accordance with BS3900: Part B (BS EN ISO33) to humid atmospheres containing SO₂ using 1 litre of SO₂ per cycle (0.33%). Each cabinet cycle was run continually for 24 hours. The test boards were exposed for four cycles. The boards were visually inspected after each cycle.

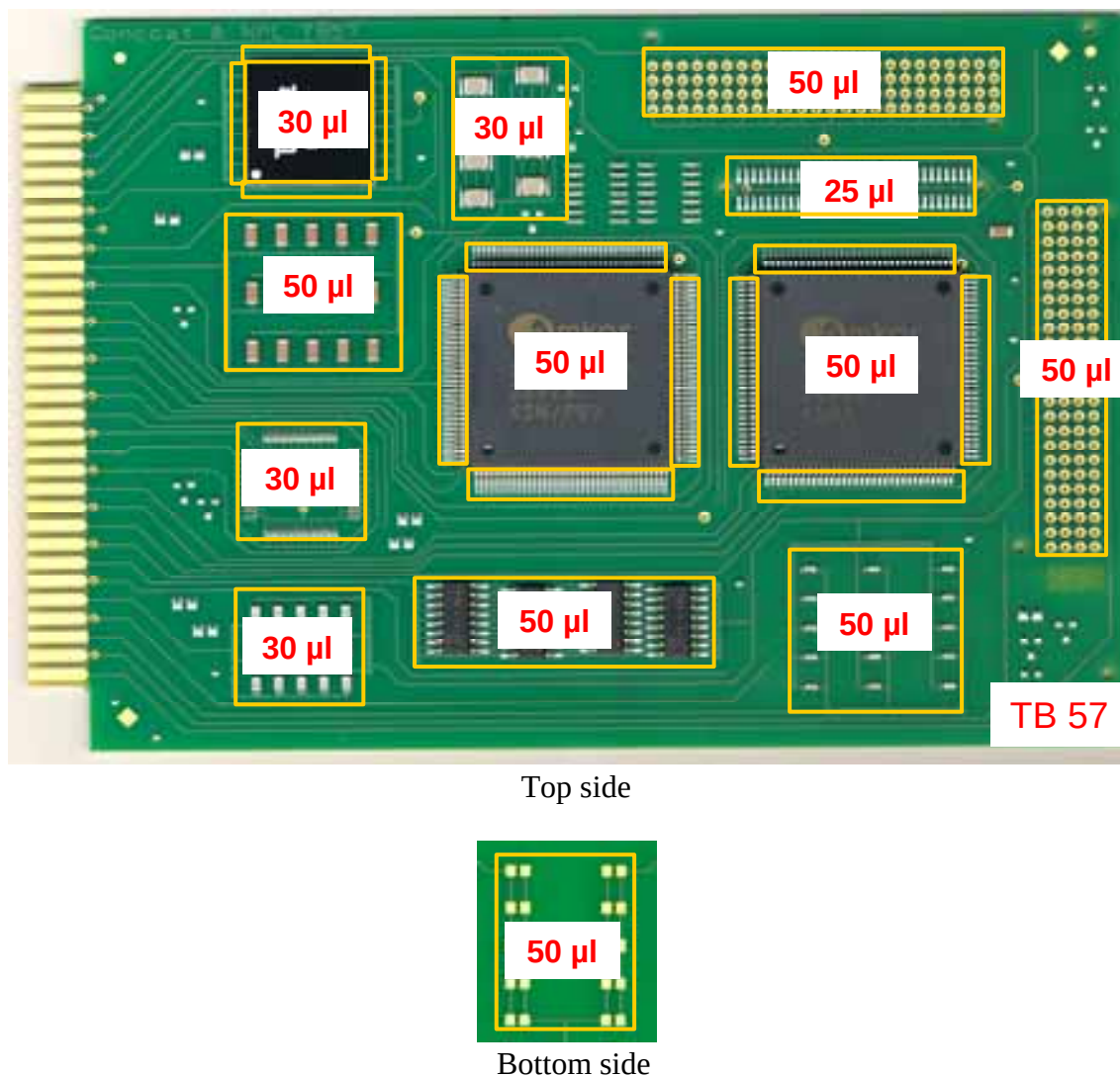


Figure A.1. Contaminant volume and contamination area for each test pattern

A.5 SURFACE INSULATION RESISTANCE MEASUREMENTS

A Gen3 Auto SIR that has a current sensitivity of 1×10^{-11} A was used to monitor the SIR values. The SIR measurements were performed according to the test procedure in Section 2.3.3. Test conditions of 40°C/93%RH with 50V bias and 85°C/85%RH with 50V bias were used to test coated assemblies and PCBs without contaminants. Test condition 40°C/93%RH with 5V bias was used to test coated assemblies with flux contaminant, and 85°C/85%RH with 5V bias was used to test coated assemblies with surfactant contaminant and PCBs with SO₂ contaminant. Test condition 85°C/85%RH was used here to check the suitability of this test condition for conformal coating.

The SIR test matrix is summarised in Table A.3. Since two TB 57 boards from each assembly process were tested for each combination of contaminant and coating, the results are presented as averages of two measurements for each test pattern. For the TB67 PCBs with the SO₂ contaminant, one board was tested for each coating, and the results are the average of four SIR measurements.

Table A.3. Matrix for SIR testing

Test board	Contaminant	SIR test parameter
TB57 assembly A	None	40°C/93% 50V
TB57 assembly B		85°C/85% 50V
TB67 PCB		40°C/93% 50V
TB57 assembly A	Flux	40°C/93% 5V
TB57 assembly B		
TB67 PCB	SO ₂ exposure	
TB57 assembly A	Surfactant	85°C/85% 5V
TB57 assembly B		

A.6 RESULTS AND DISCUSSION

A.6.1 Coating thickness on assemblies

The work in an earlier phase³ showed that coating coverage played an important role in the protection performance. The test assembly in this work was assembled using a wide range of components, and the coating coverage on different components was inevitably different. Even on one component type the coating thickness at different positions was not same. The coating thickness on components cannot be simply checked due to the transparency of the coating. Here the coating thickness for the QFP leads (Pattern F) and the copper track from each coating were assessed by micro section, as illustrated in Figure A.2. Since the fluoroacrylate coating was about 1µm thick it is not included in Figure A.2. The section position for QFP leads was at top end of the leads, as shown in Figure A.3, position 1. The images clearly show that the silicone coating was much thicker than the others, and the double dip coatings were thicker than single dip.

The coating sections are important and it is noteworthy that the coverage of the coatings on the QFP leads is much thinner than that on the PCB copper tracks. Figure A.2 shows that there was hardly any coating on top of QFP leads for most coatings, and in this area only a very thin coating can be observed on the silicone single coating, which thickens slightly for the double dip coatings. Therefore double dip coating process improves the coating coverage on sharp edge leaded components. Coating thickness was found to vary at different positions for one component type. The QFP leads (Pattern F) with polyurethane coating were polished with silicon carbide paper to four positions. The coating thickness at four positions is shown in Figure A.3. The coating thickness became thicker, and the coating increasingly covered the top of leads as the component body is approached.

QFP leads



Copper track



Water-based acrylic (1)



Solvent-based acrylic



Water-based acrylic (2)



Water-based acrylic (2) –Double dip



Polyurethane



Silicone



Silicone-Double dip

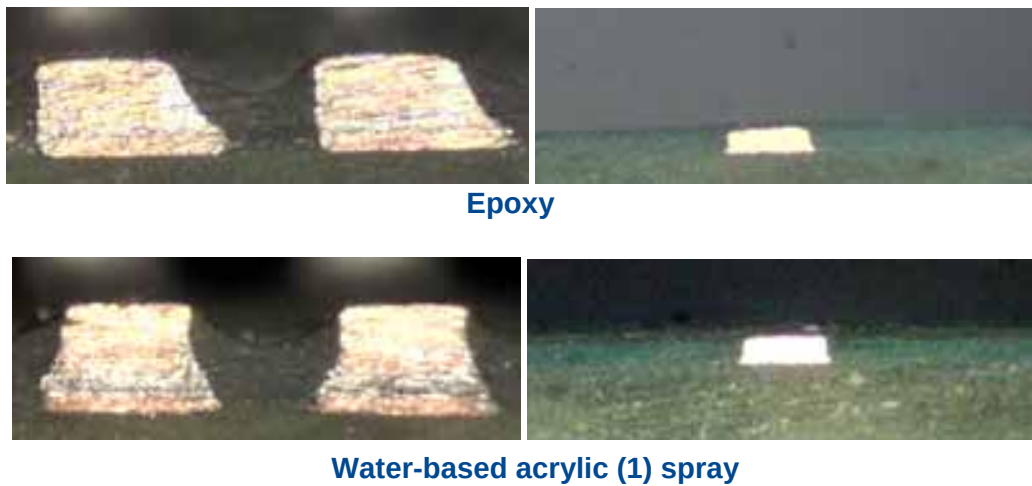


Figure A.2. Thickness of coatings on QFP leads and copper tracks

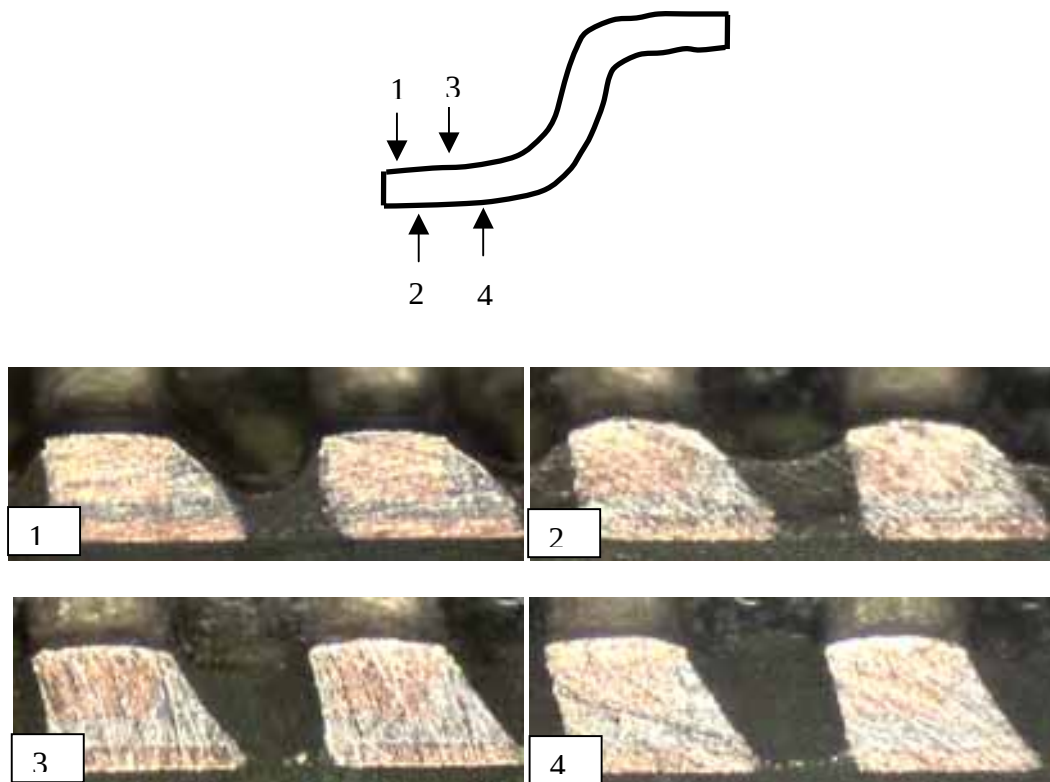


Figure A.3. Coating thickness on QFP leads with polyurethane coating

A.6.2 Effect of flux residues from assembly process on SIR results

The values of SIR with time on un-coated bare PCBs, A assembly and B assembly are presented in Figure A.4, and the final SIR results from the two assemblies are summarised and compared with the bare PCBs in Figure A.5. Three comb patterns underneath the QFPs, G, K and I were not solder paste printed, and three wave soldering components were not processed. These patterns are shown on following charts by bars drawn in the shadow mode. The solid bars show test patterns that were printed with solder paste. The figures clearly show that the SIR values on A assembly were marginally lower than that of B assembly, which were in turn lower than that of the bare PCBs, for patterns printed with solder paste. This implies that assembly process from both manufactures left some residues, lowering the SIR particularly for fine pitch component patterns. For the assembled boards on patterns without paste the SIR values were slightly higher than that on bare PCBs. This suggests that the high temperature reflow process helped to clean the boards. The differences in the SIR values between different test patterns were due to their different pitch and ohm squares⁶. As expected the fine pitch test patterns with high ohm squares gave low SIR values, and the coarse pitch test patterns with low ohm squares gave high SIR values.

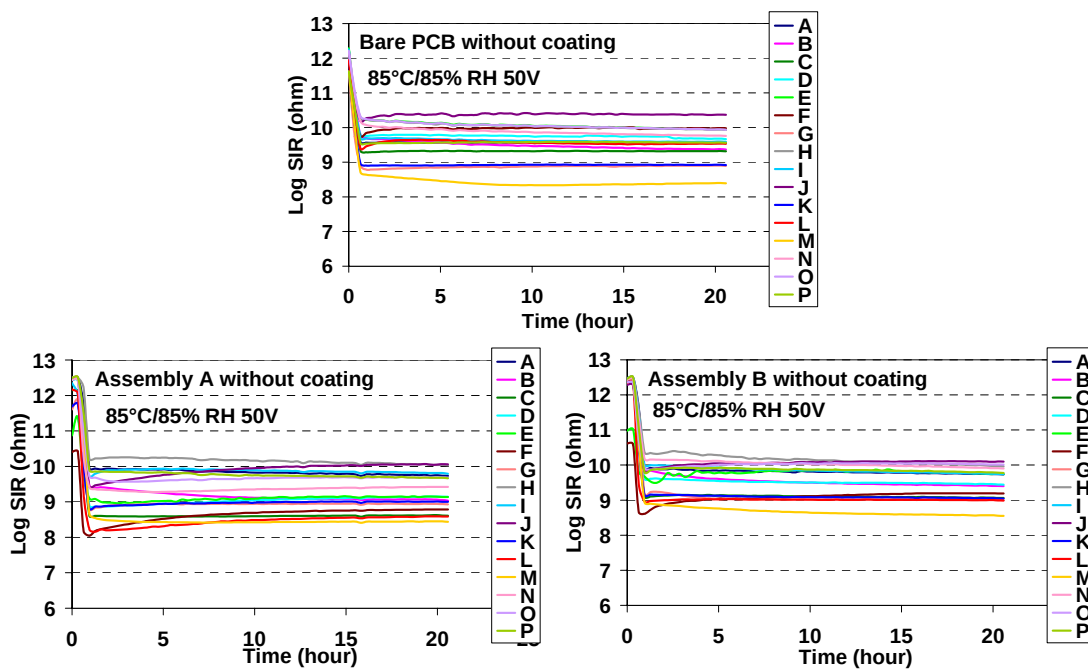


Figure A.4. SIR plots for the un-coated PCB, A assemblies and B assemblies

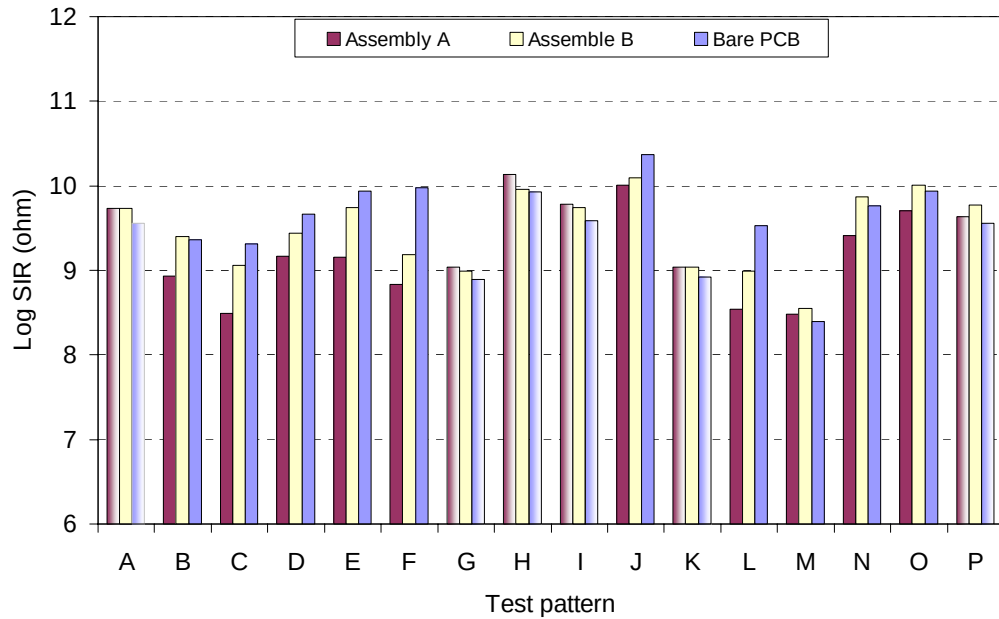
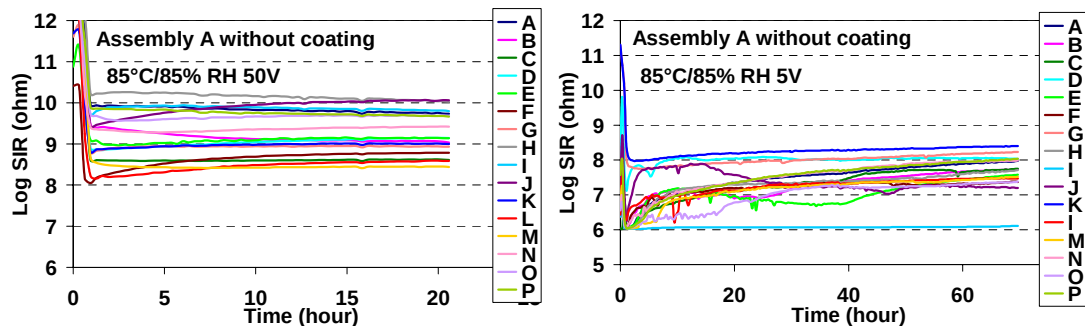
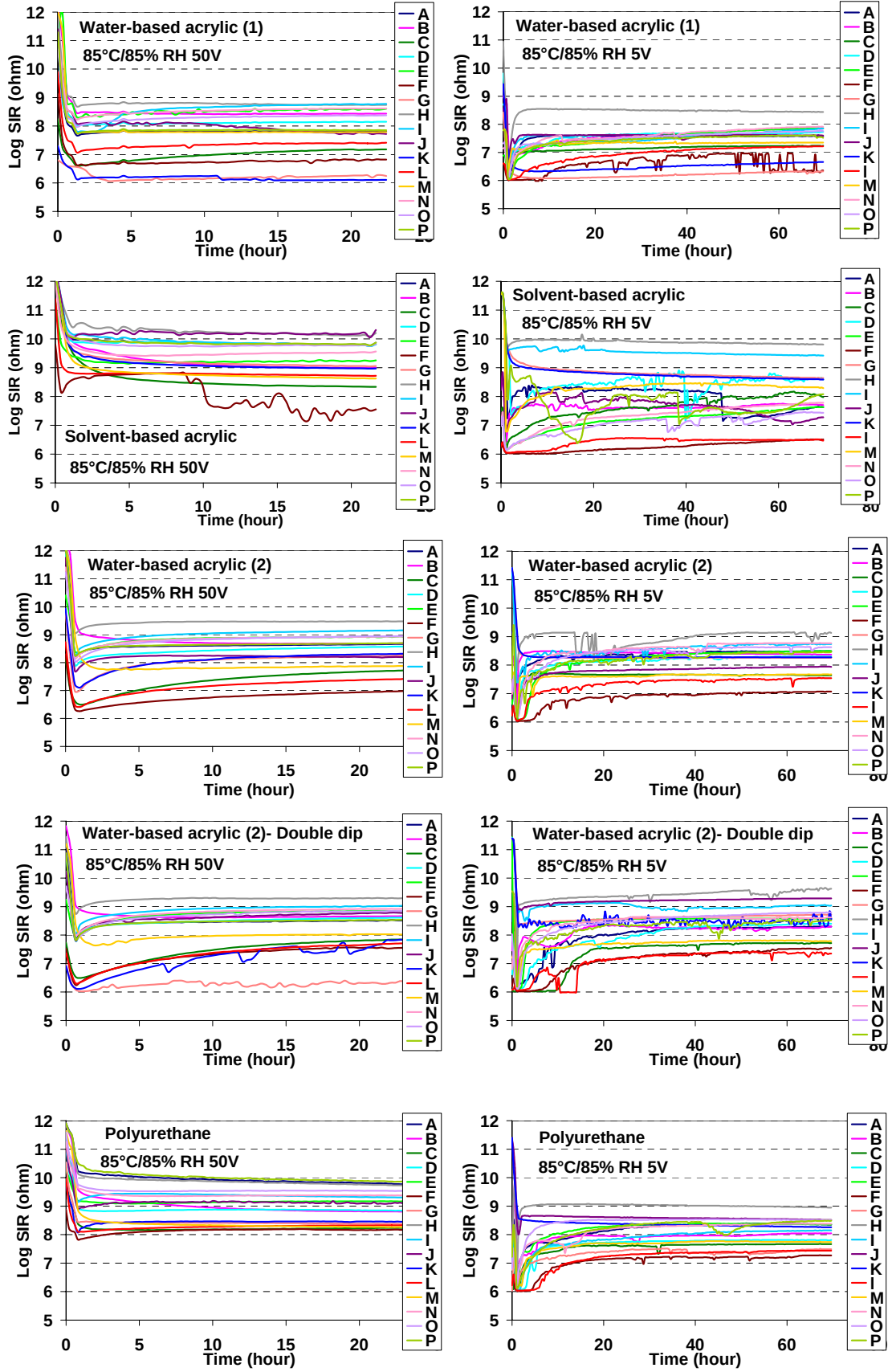


Figure A.5. Final SIR values for the un-coated PCB, A assemblies and B assemblies

A.6.3 Effect of contamination from harsh environments on SIR results

The variation of SIR values with time on coated A assemblies (TB57) before and after contamination with surfactant are presented in Figure A.6, and similar results for B assemblies are presented in Figures A.7. Similarly the results for assemblies contaminated with flux are presented in Figures A.8 and A.9, and the results for coated PCBs (TB67) before and after SO_2 exposure are showed in Figure A.10. The SIR results on uncontaminated assemblies and PCBs are included in the left hand side of the figures for comparison. The results presented in the figures are an average from two assemblies and one PCB (four test patterns) for each combination. It is evident from these figures that the SIR measurement with the new TB57 design test board was very sensitive in the degree of protection of the different coating types with each contaminant. These results are discussed in following section.





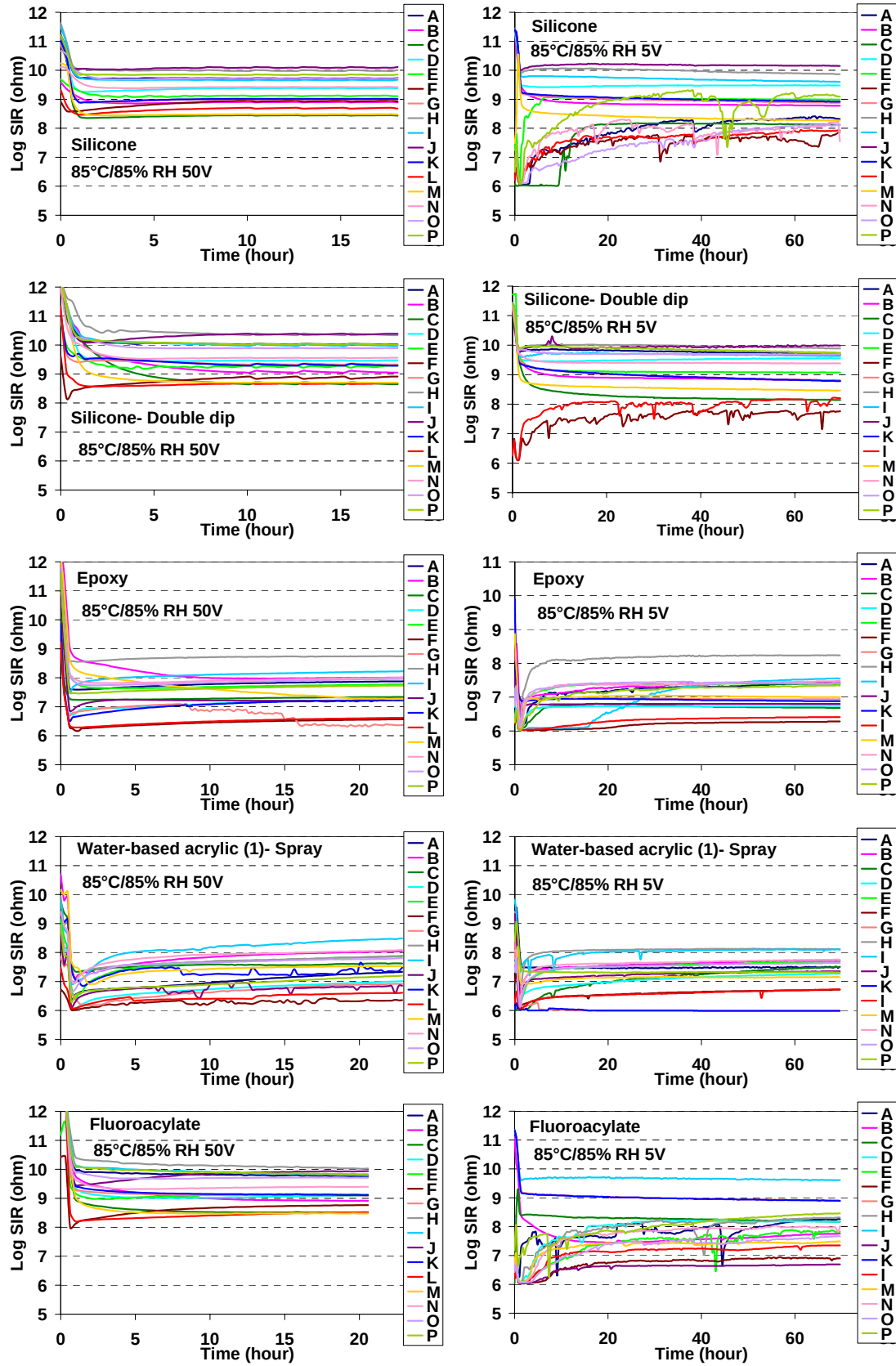
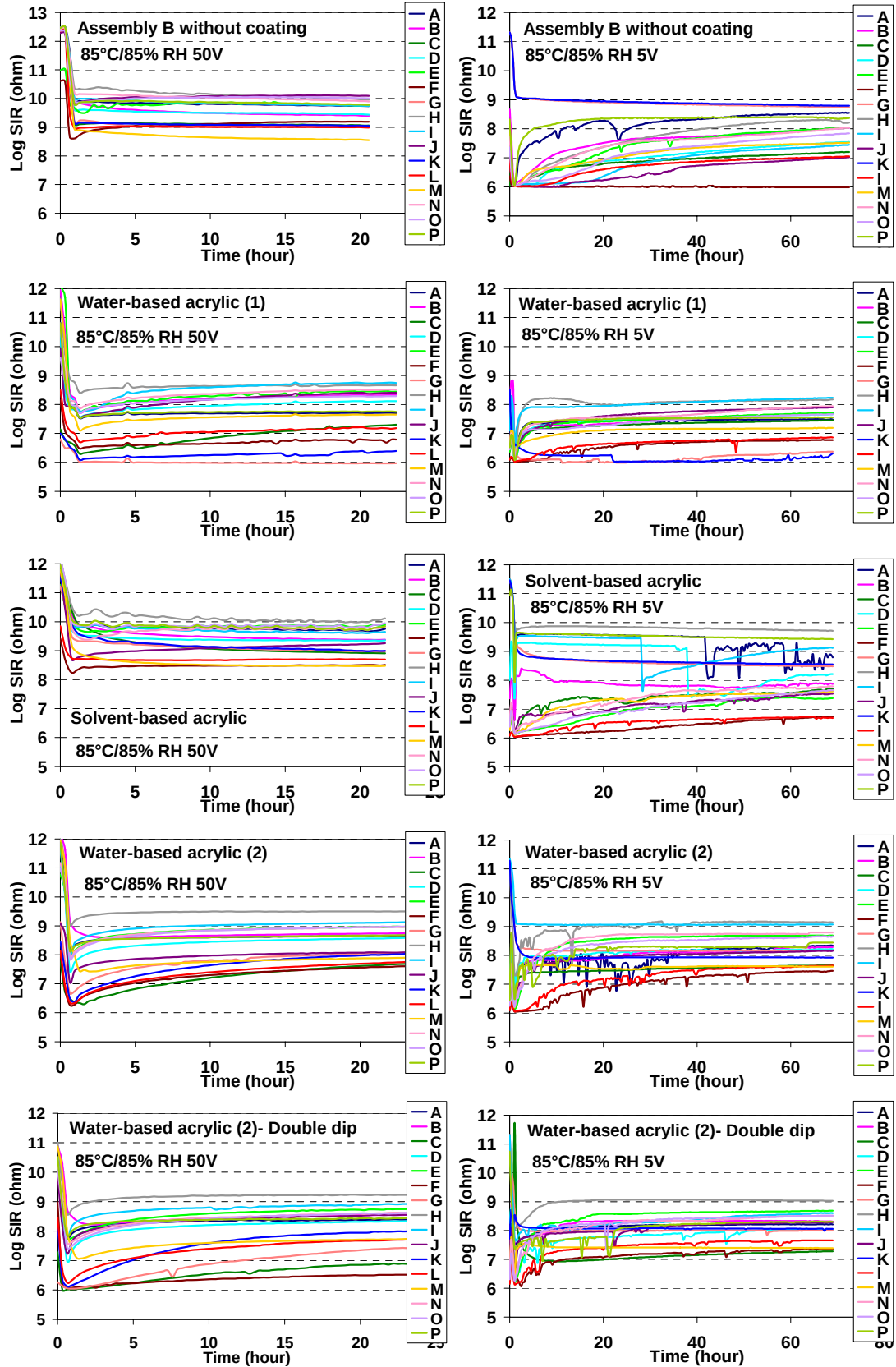
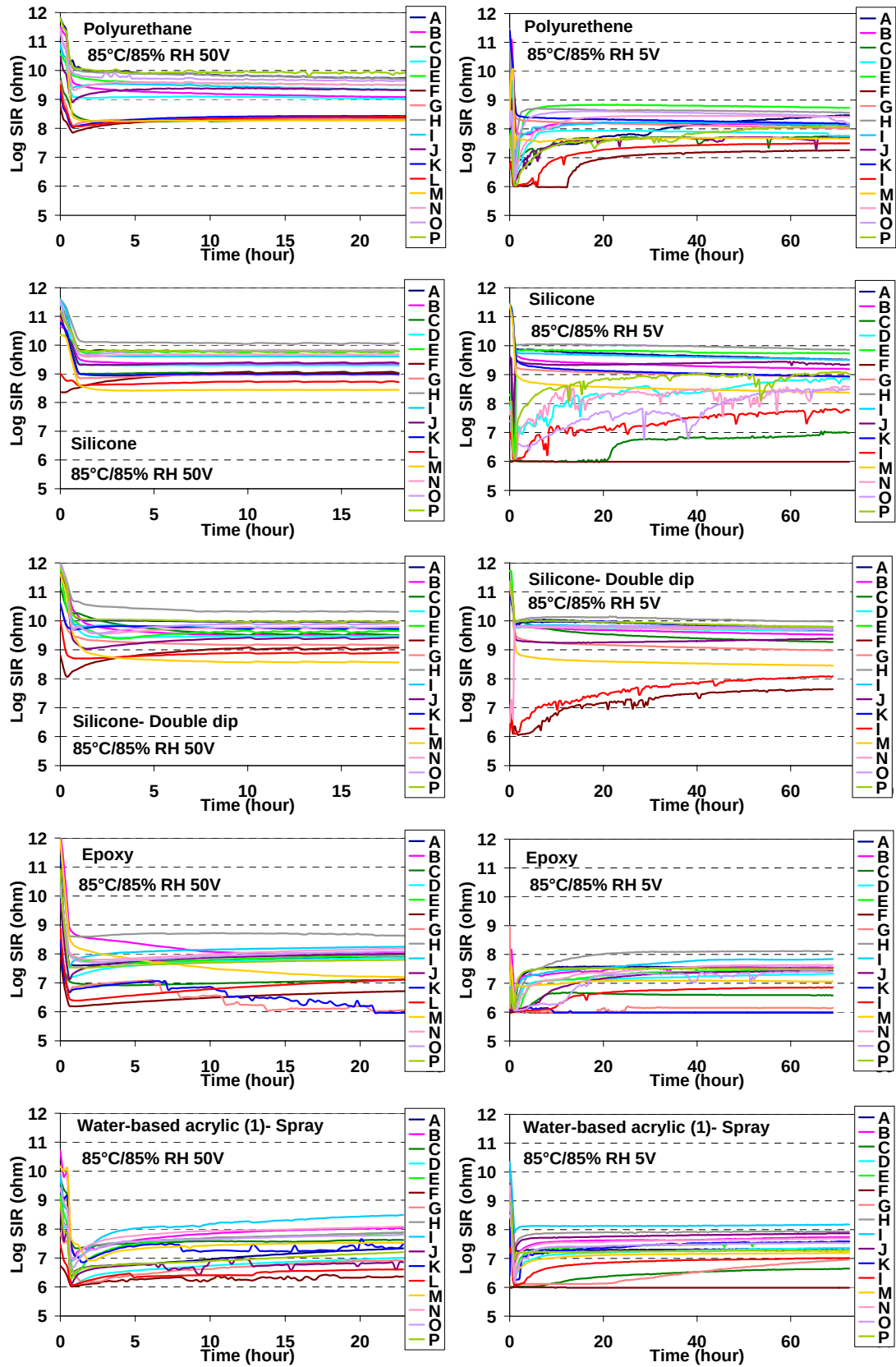


Figure A.6. SIR plots for different coatings with surfactant on A assemblies





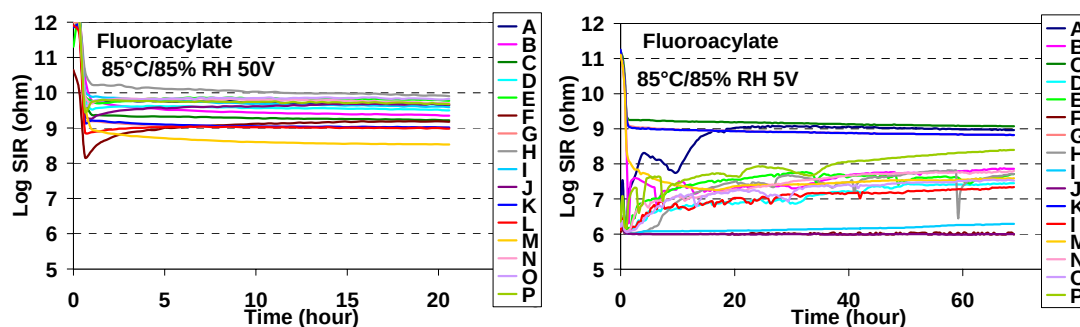
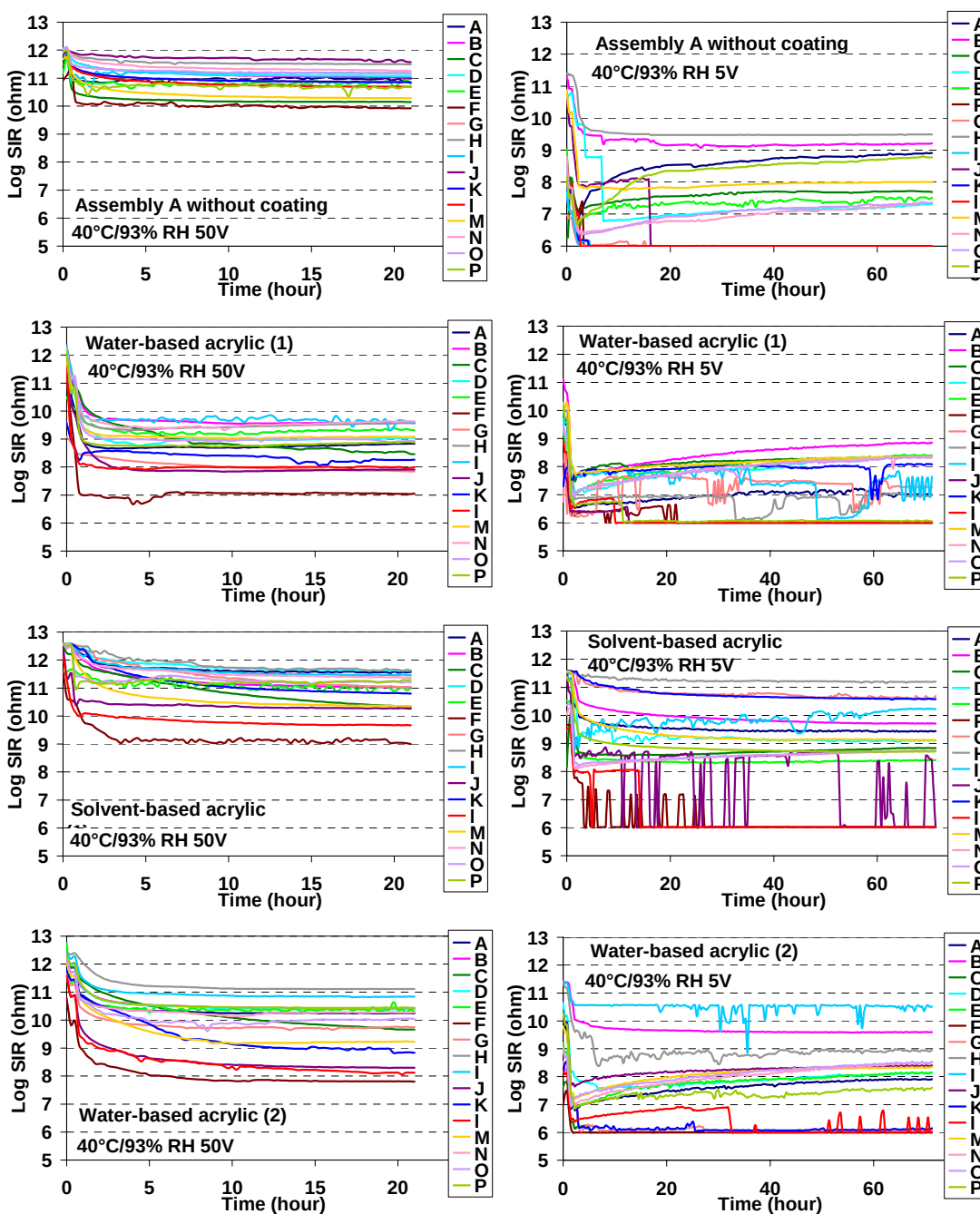
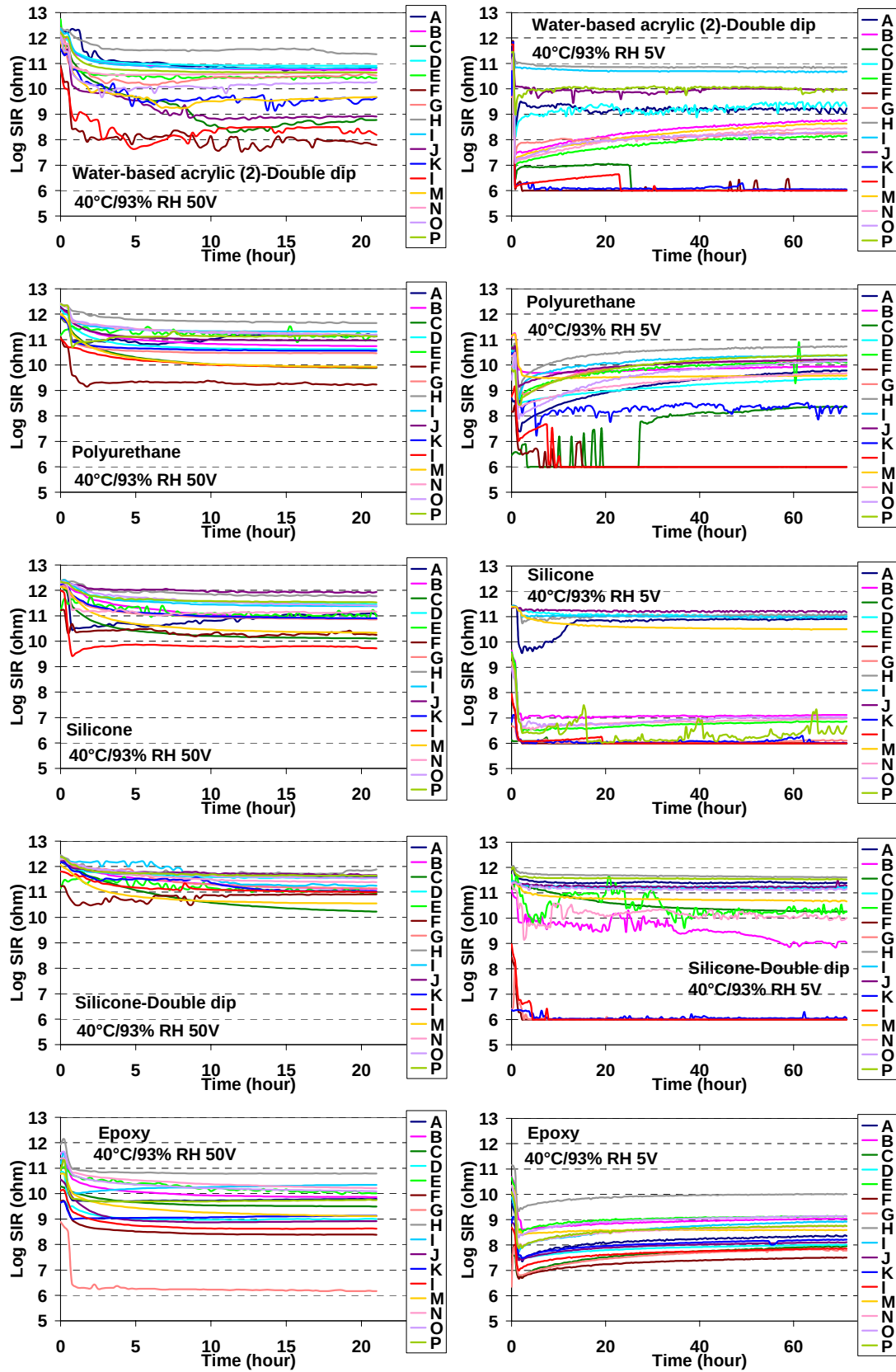


Figure A.7. SIR plots for different coatings with surfactant on the B assemblies





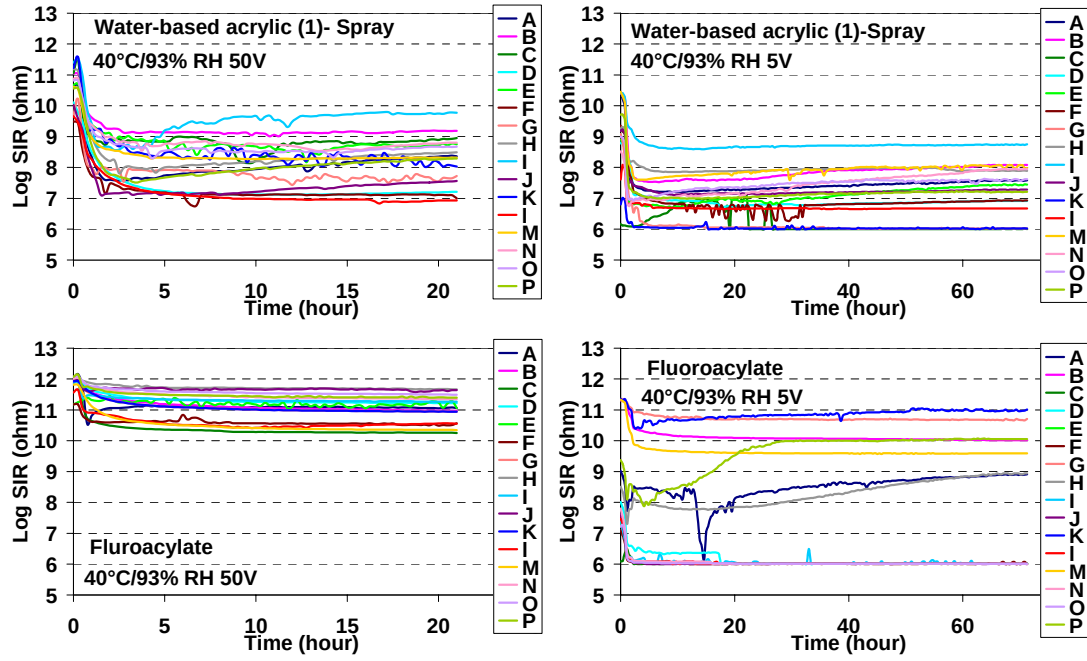
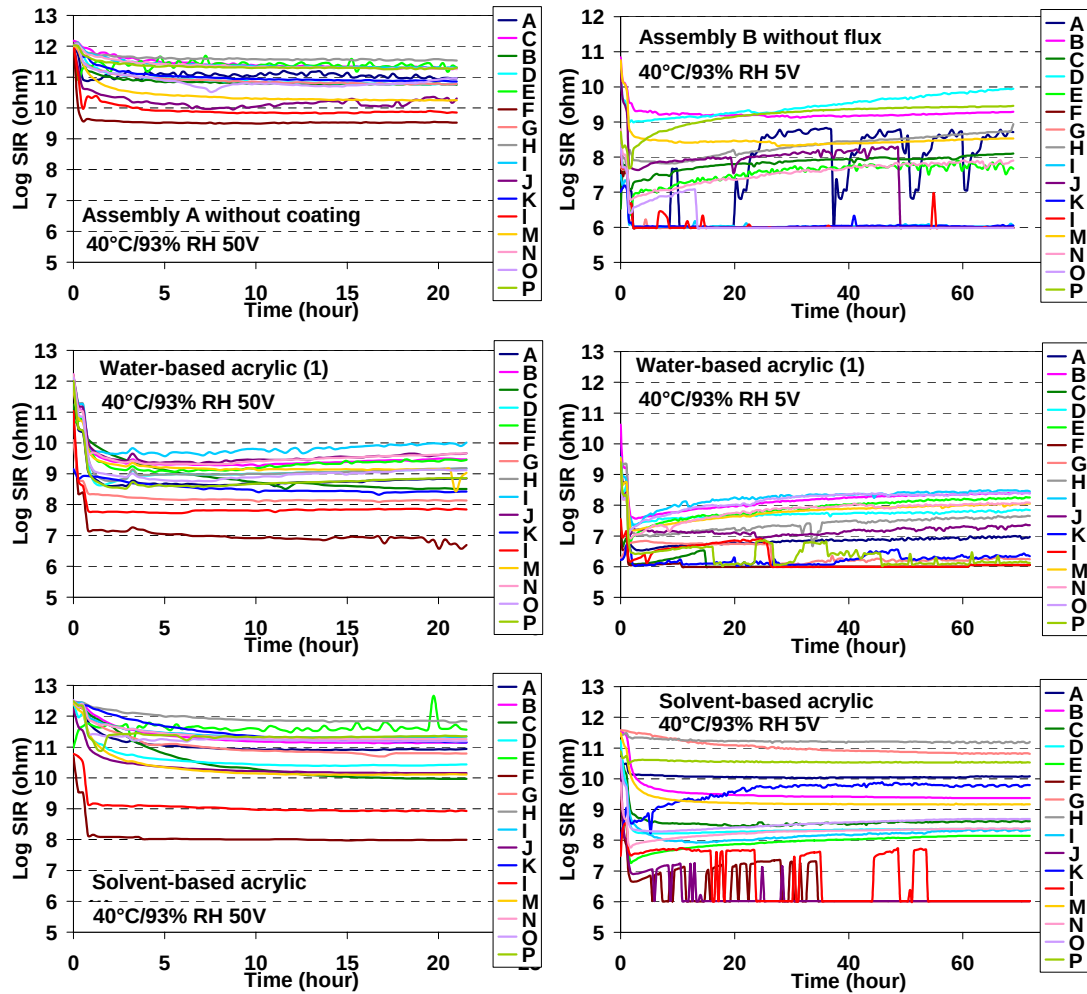
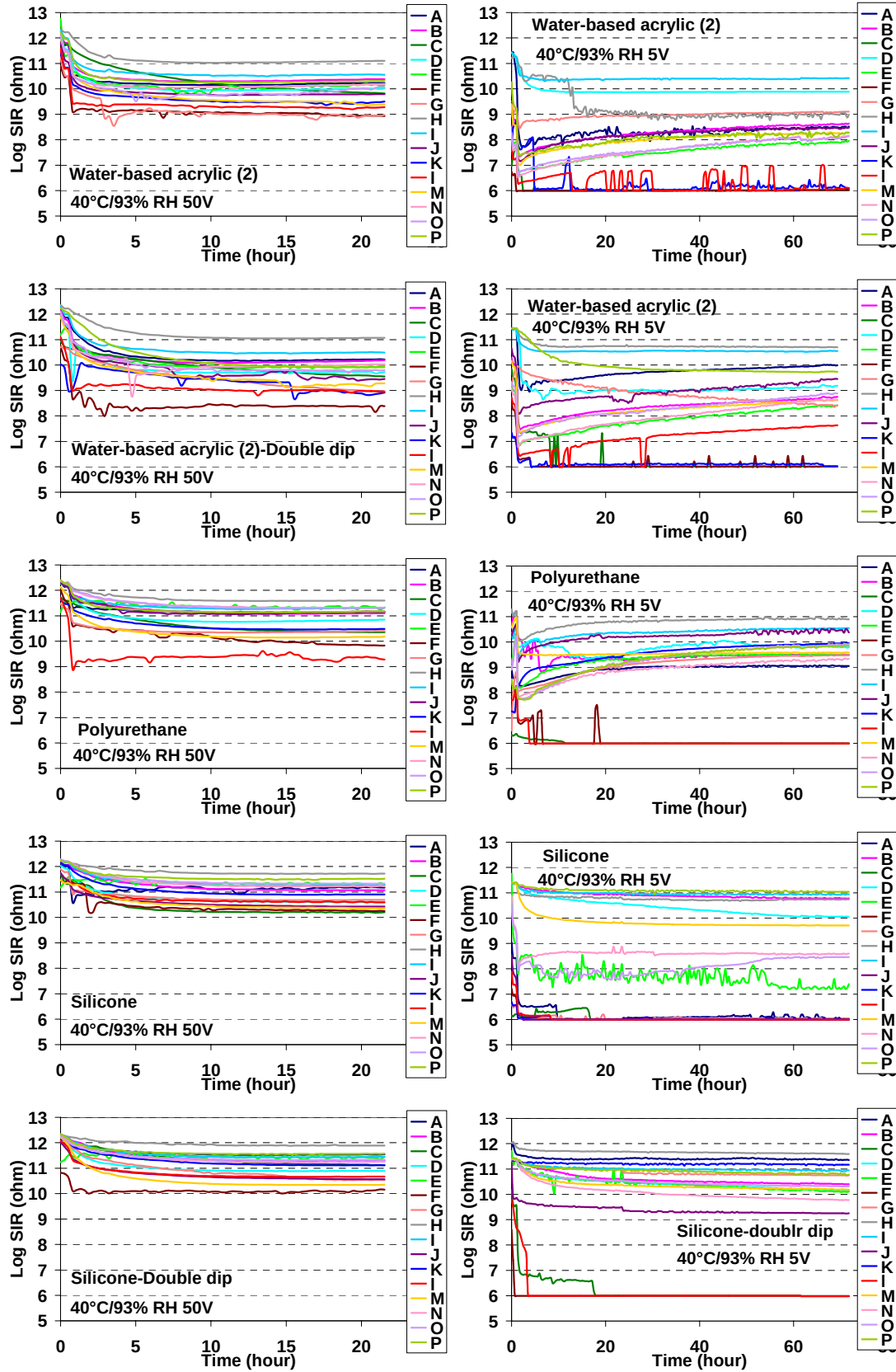


Figure A.8. SIR plots for different coatings with flux on the A assemblies





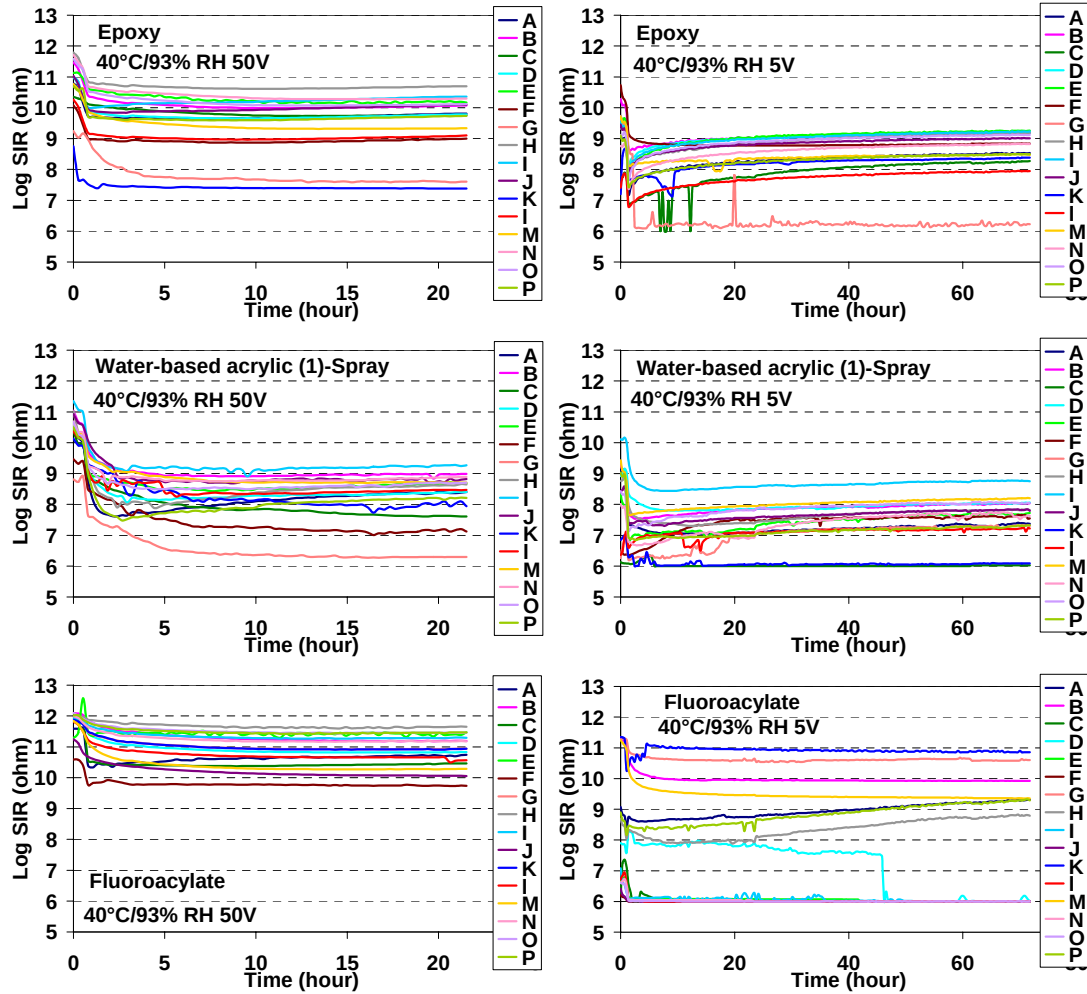


Figure A.9. SIR plots for different coatings with flux on the B assemblies

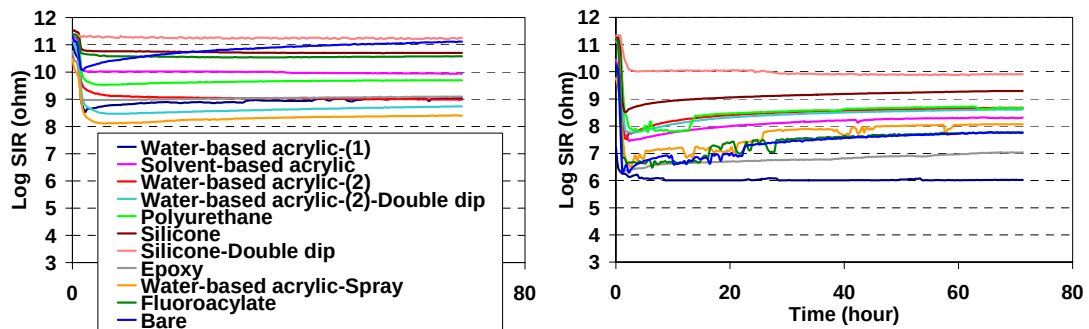


Figure A.10. SIR plots for different coatings on PCBs exposed SO₂

A.6.3.1 Effect of contaminants on coating protection performance

The average final SIR values from all test patterns on different coatings are plotted in Figure A.11 for the A assemblies with surfactant, and the log SIR change before and after contamination for this combinations are summarised in Figure A.12. Similarly the results for the B assemblies with surfactant are in Figures A.13 and A.14, the A assemblies with flux in Figures A.15 and A.16, and the B assemblies with flux in Figures A.17 and A.18, and for the PCBs exposed to SO₂ the results are in Figures A.19 and A.20.

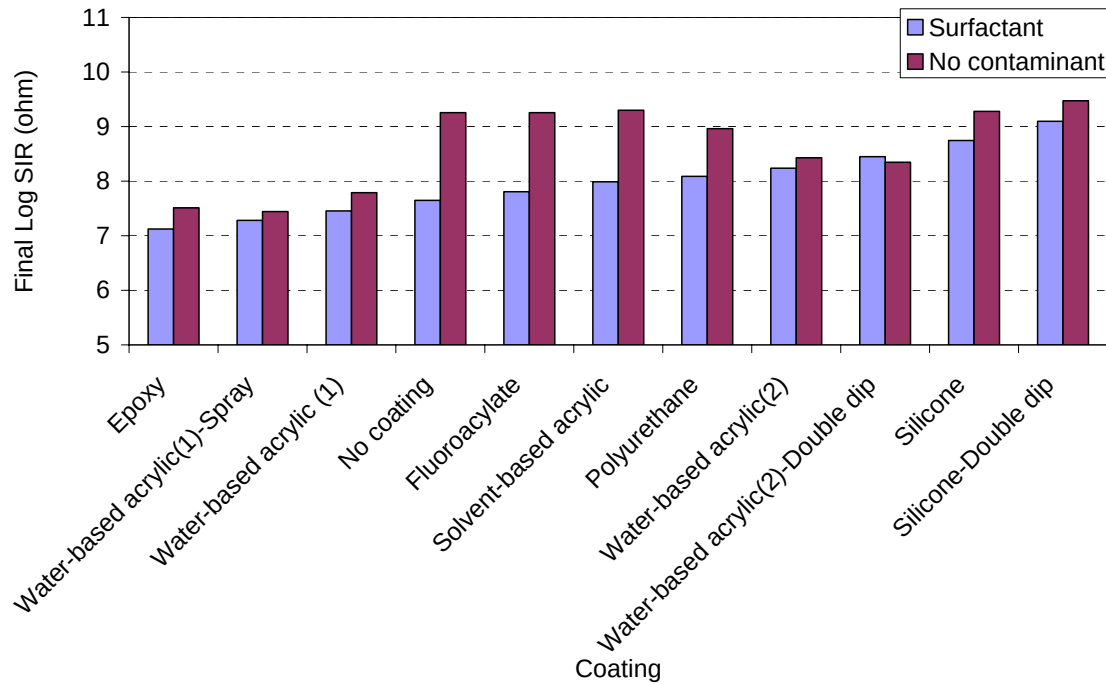


Figure A.11. Final SIR values for different coatings with surfactant on the A assemblies

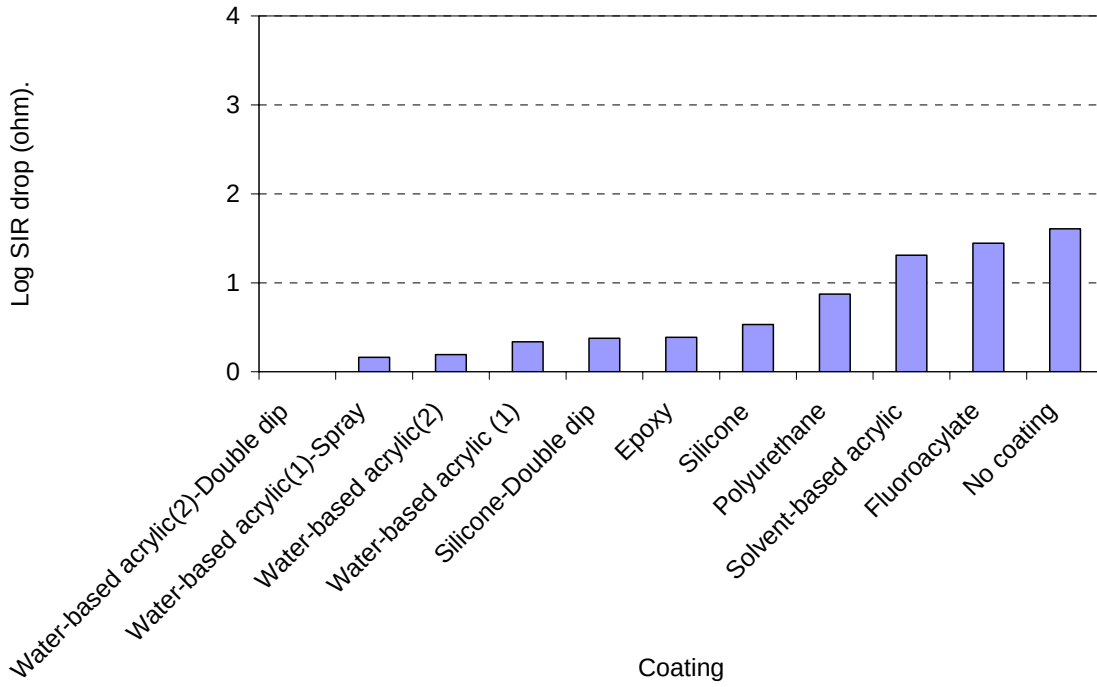


Figure A.12. Final SIR drop after surfactant contamination on the A assembly

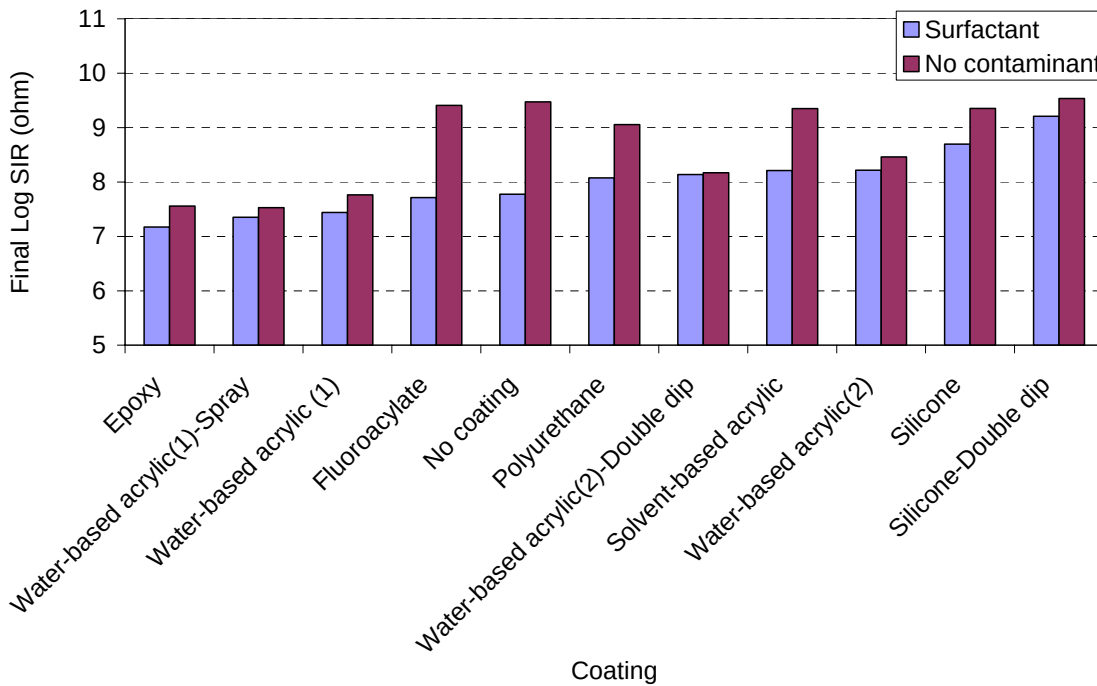


Figure A.13. Final SIR values for different coatings with surfactant on the B assemblies

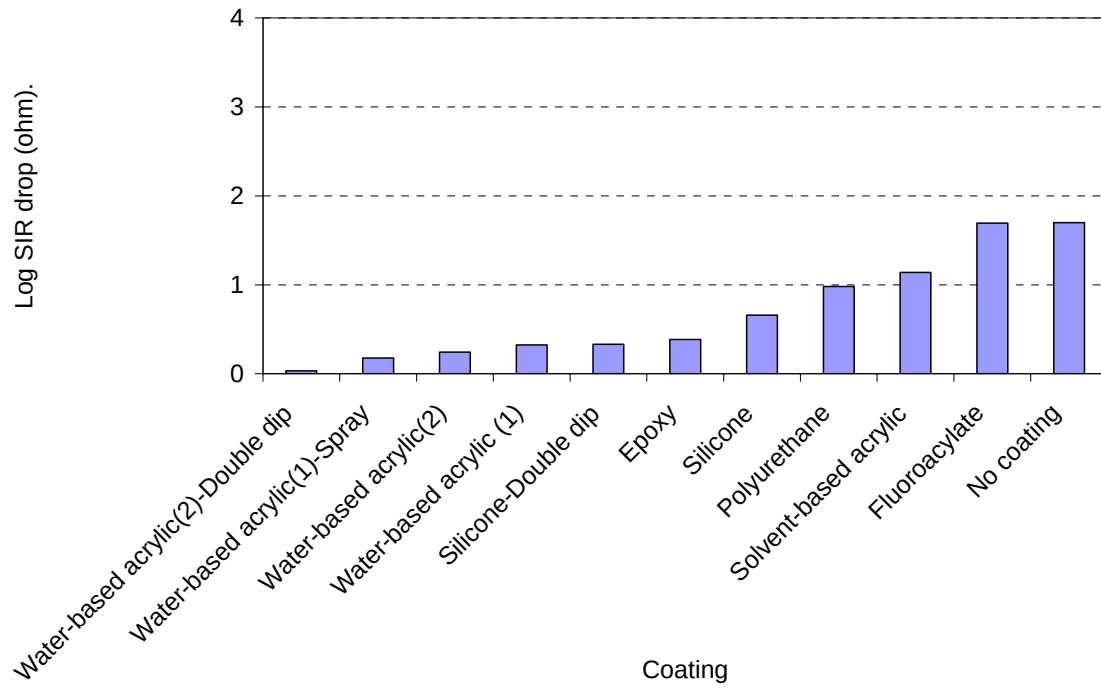


Figure A.14. Final SIR drop after surfactant contamination on the B assemblies

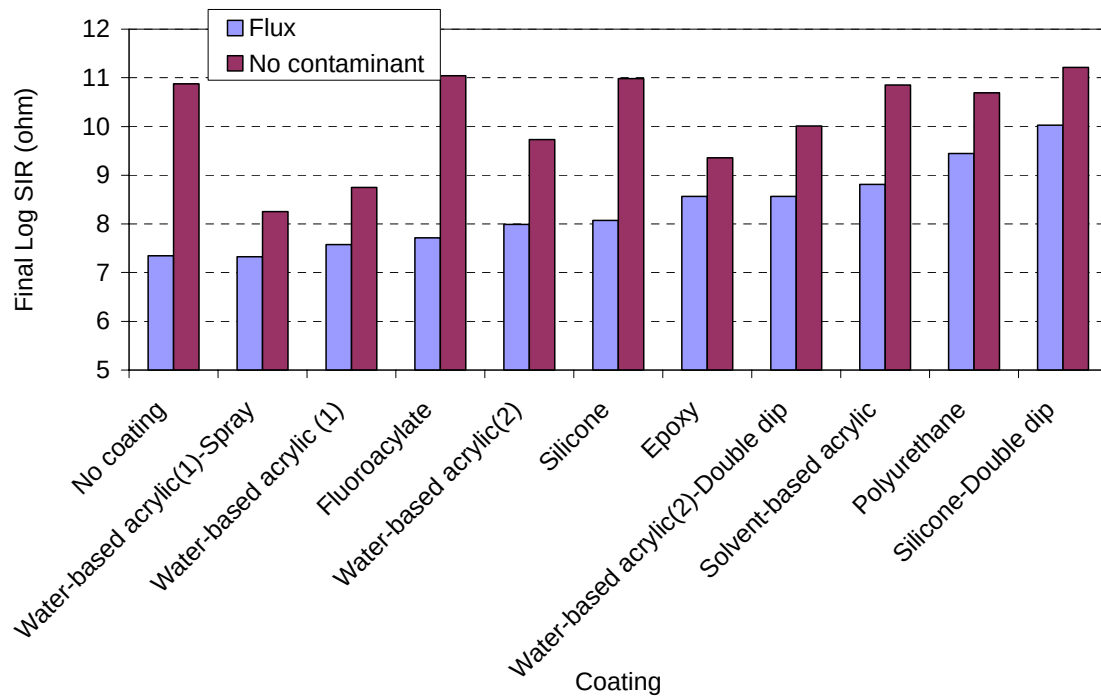


Figure A.15. Final SIR values for different coatings with flux on the A assemblies

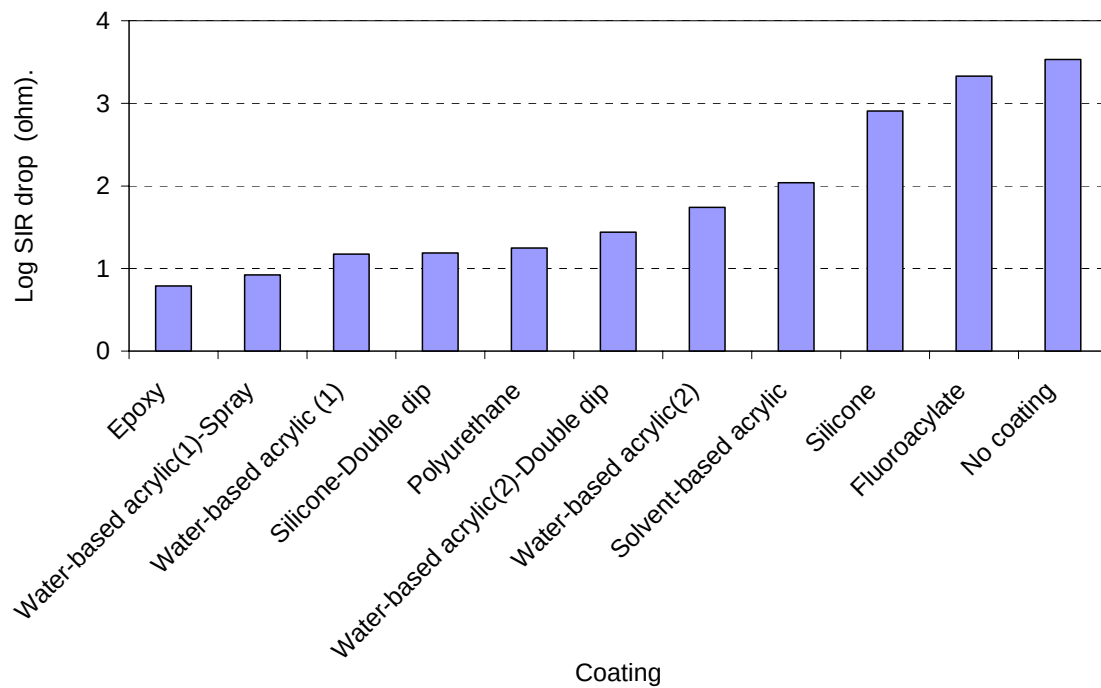


Figure A.16. Final SIR drop after flux contamination on the A assemblies

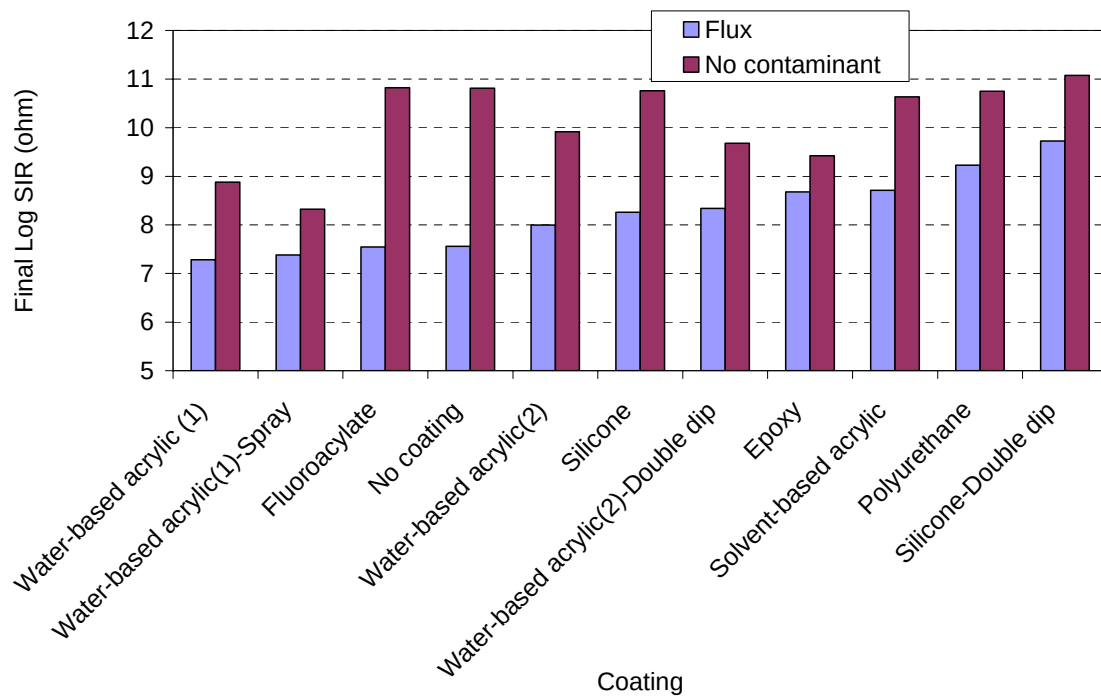


Figure A.17. Final SIR values for different coatings with flux on B assemblies

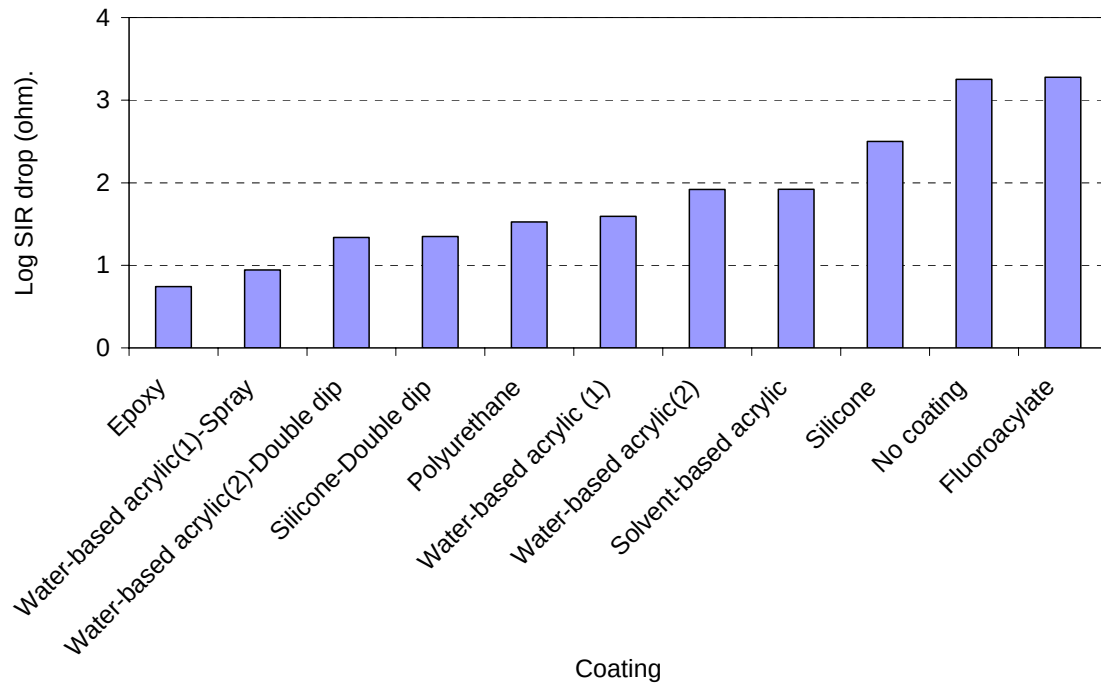


Figure A.18. Final SIR drop after flux contamination on B assemblies

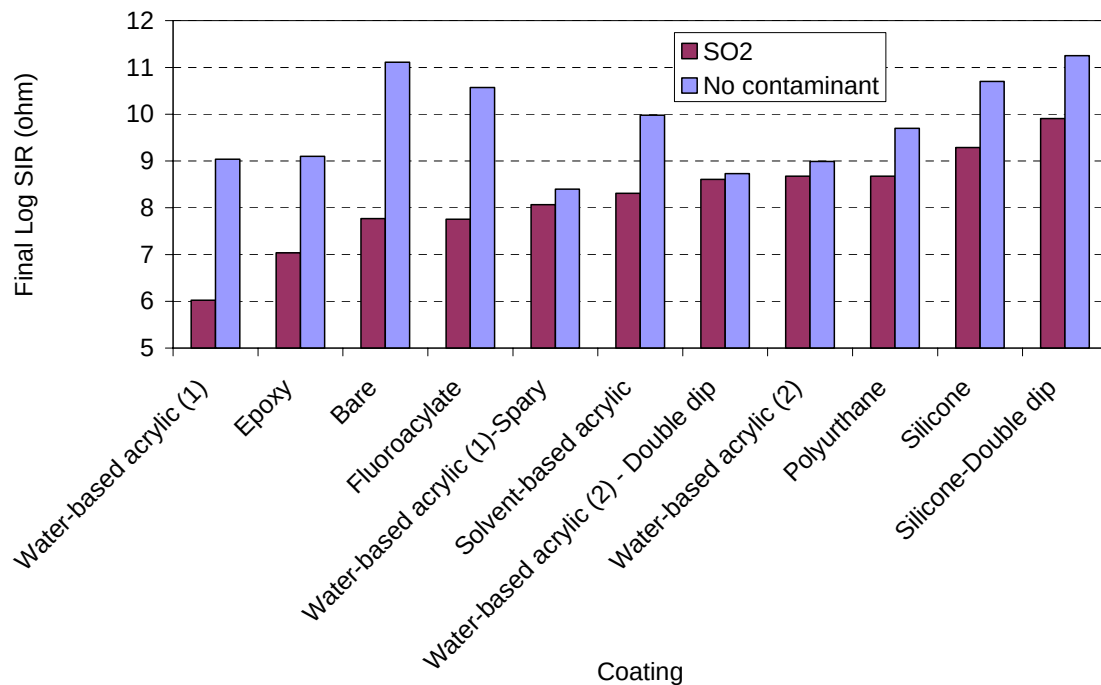


Figure A.19. Final SIR values for different coatings on PCBs exposed to SO₂

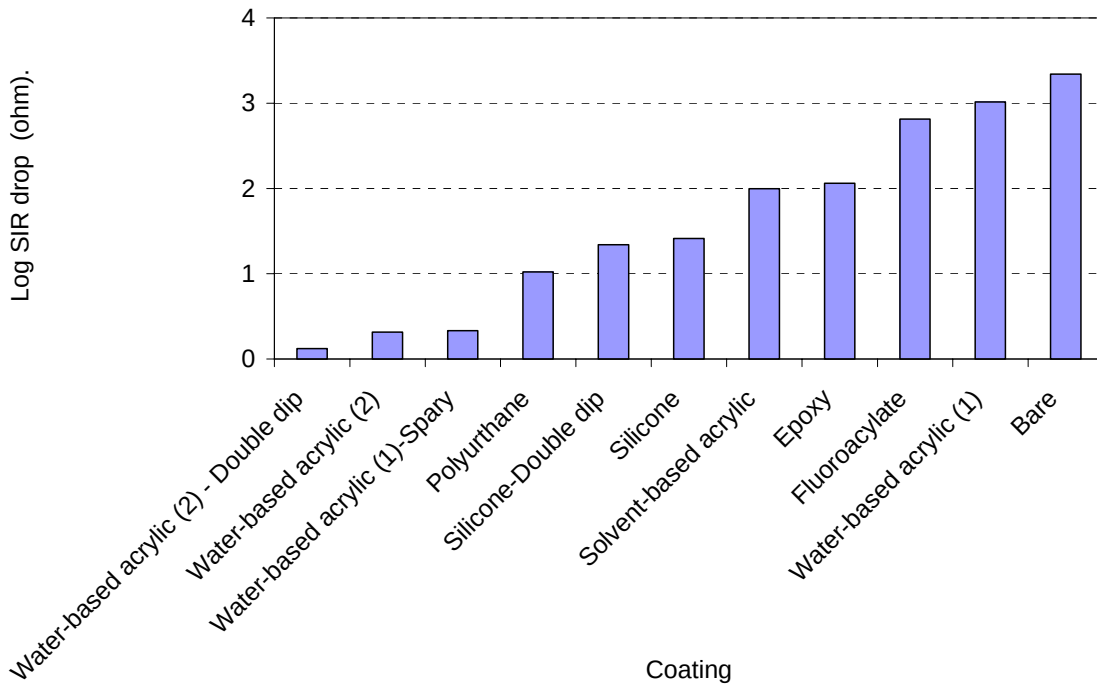


Figure A.20. Final SIR drop after SO₂ exposure on PCBs

There are some important points to note from these results:

- Coatings differed on the protection different level for the underlying electronic circuit.
- A low final Log SIR value does not necessarily mean the coating was permeable to the contaminant, as each coating has a different level of moisture permeability, which will affect its results under the test condition. The final log SIR values without contaminants in the figures reflect moisture permeability of different coatings. Therefore the Log SIR changes before and after contamination should be more representative of contaminant permeation. However the final Log SIR value provides a direct evaluation of the electrical reliability of the circuit underneath the coatings.
- Compared with the uncoated assembly, all the coatings provide a semi-permeable barrier to reduce the contaminant level reaching underlying circuit, The SIR drop for all coatings was lower than that for the uncoated boards, as seen in Figures A.10, A.12, A.14 and A.16. However reducing the contamination reaching the underlying circuitry is not necessarily the most important point, since some coatings have high water permeability, lowering the SIR value and degrading reliability. Therefore if a coating is going to be used in humid conditions, then water permeability should be taken into count, and the final log SIR value should be used to evaluate coating protection performance, and not only the SIR drop.
- The protection level as measured by the final SIR depends on coating material and contaminant type. For surfactant contamination, the silicone coating

provided the highest degree of protection for underlying circuit, and the epoxy was the poorest with respect to the final SIR. For flux contamination, the polyurethane coating offered the highest degree of protection, and water-based acrylic (1) is the poorest. For SO₂ exposure, the silicone was the best and water-based acrylic (1) was the poorest. Over all the silicone double dip gave the highest final SI, and hence the best protection against all contaminants.

- The SIR drop results for surfactant contamination show that the two water-based acrylic coatings showed smaller SIR drop than other coating types, but this does not necessarily indicate that the water-based acrylic coatings has a low permeability for surfactant. The surfactant results were influenced by using the test condition, 85°C/85%RH with 50V test bias, water permeability of coating more dominant than for 40°C/93%RH. The SIR results will therefore be lower for more water permeable coating. Hence the SIR drop for the more water permeable water-based acrylic coatings was not as significant after surfactant contamination. For the flux contamination epoxy coating produced the smallest SIR drop, and for SO₂ exposure the water based acrylic (2) coating gave the smallest SIR drop.
- The SIR drop after contamination for double dip coatings was less than for the single dip ones, but the double dip coatings did not always give the highest final SIR. This suggest that thick coatings can help to reduce the contaminants to reach the circuit, but thick coatings will increase the total water absorption for coatings with high water permeability, which lowers the SIR.
- Temperature and humidity clearly necessary to reduce the SIR and drive the corrosion process, and not surprisingly the 85°C/85%RH test condition was the more severe test, and gave lower SIR values, than the 40°C/93%RH, as shown for the coated boards without contamination. Some fine pitch test patterns showed very low SIR values, <10⁸ ohms for the water-based acrylic and epoxy coatings. Hence the 85°C/85%RH condition was not recommended for coating performance testing. The 40°C/93%RH proved to be a more discriminating test condition, giving a wide spread of results. Therefore the 40°C/93%RH with 5V bias is suggested for contaminated boards, and the 40°C/93%RH with 50V should be used for uncontaminated boards to increase equipment sensitivity limit.

A.6.3.2 Effect of component on coating protection performance

The average final SIR values from all coatings from the different test patterns are plotted in Figure A.21 for the A assemblies with surfactant, and the SIR drop are summarised in Figure A.22. Similar plots for the B assemblies with surfactant are presented in Figures A.23 and A.24. Again the A assemblies contaminated with flux in Figures A.25 and A.26, and the B assemblies contaminated with flux in Figures A.27 and A.28.

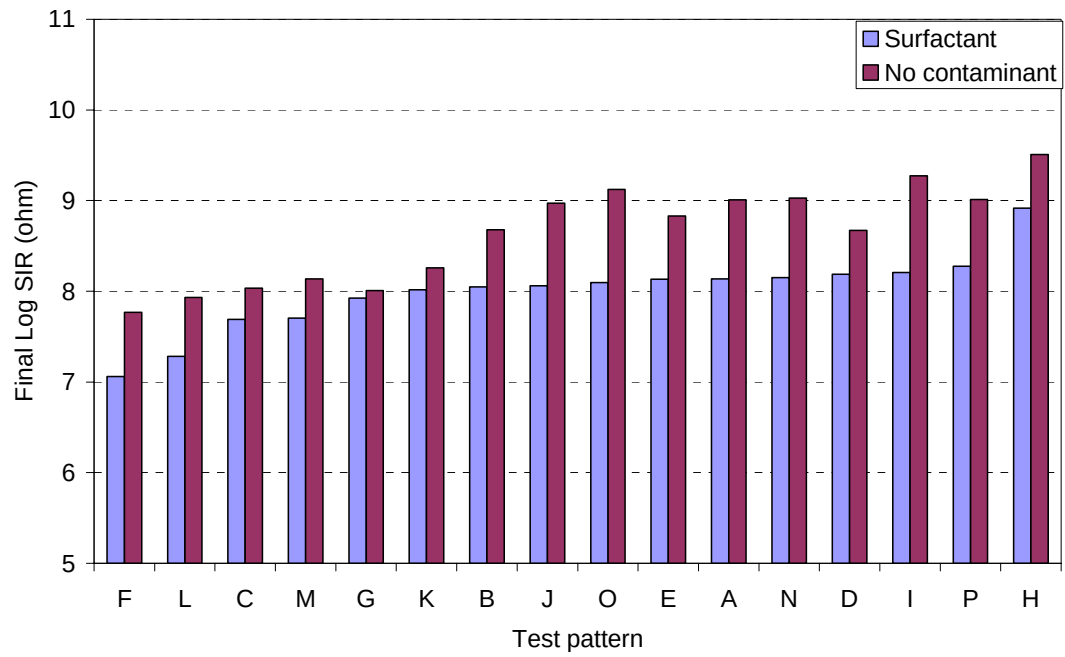


Figure A.21. Final SIR values for different test patterns with surfactant on the A assemblies

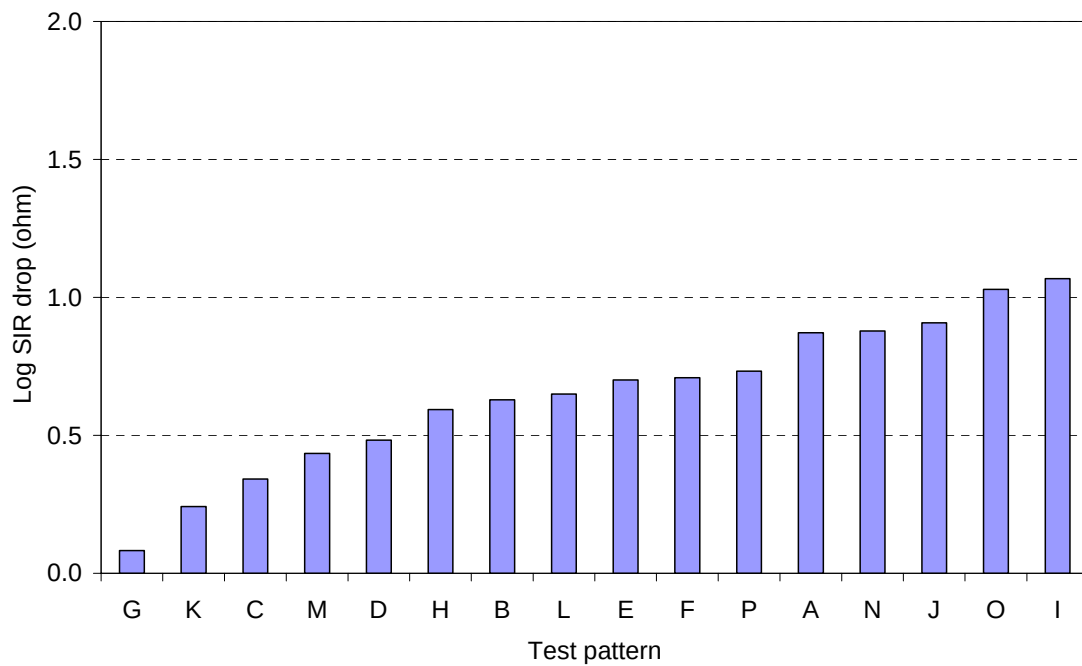


Figure A.22. Final SIR drop after surfactant contamination on the A assemblies

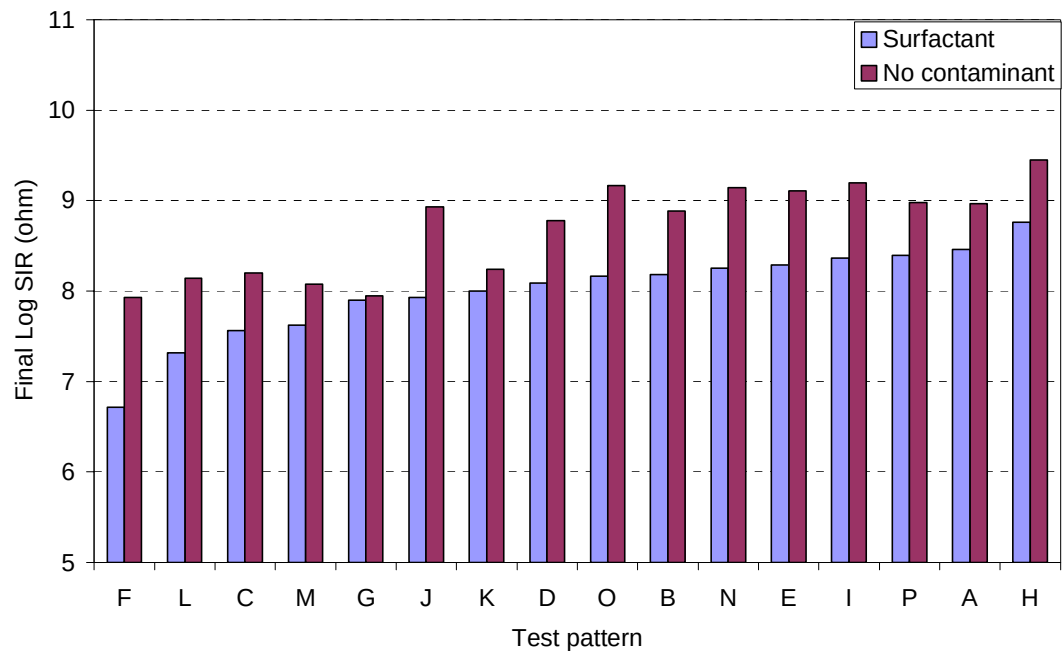


Figure A.23. Final SIR values for different test patterns with surfactant on the B assemblies

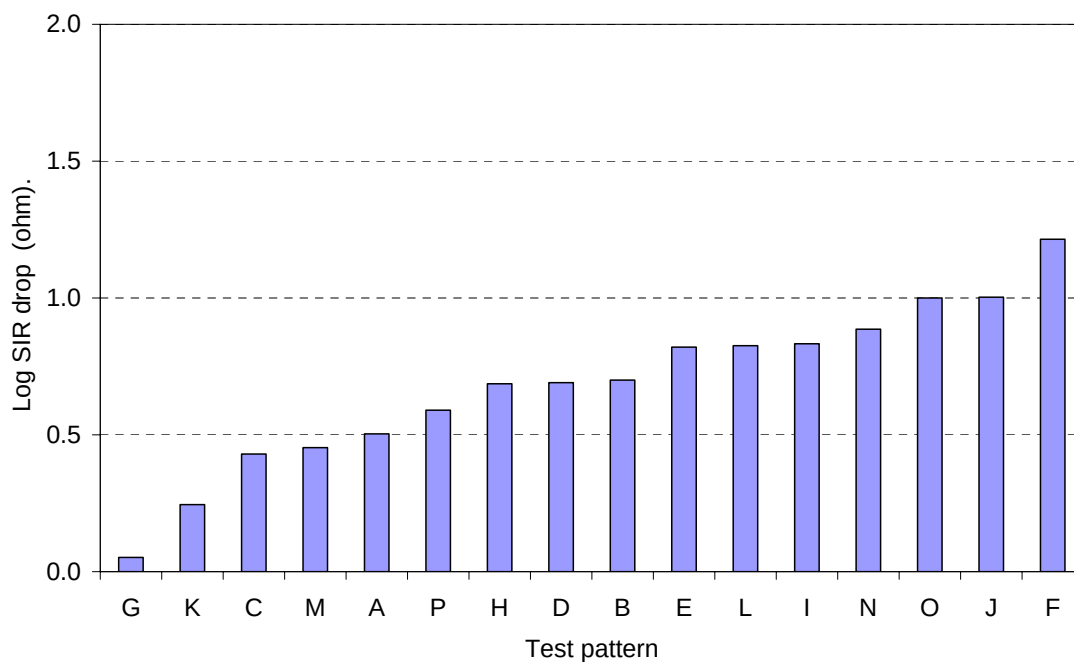


Figure A.24. Final SIR drop after surfactant contamination on the B assemblies

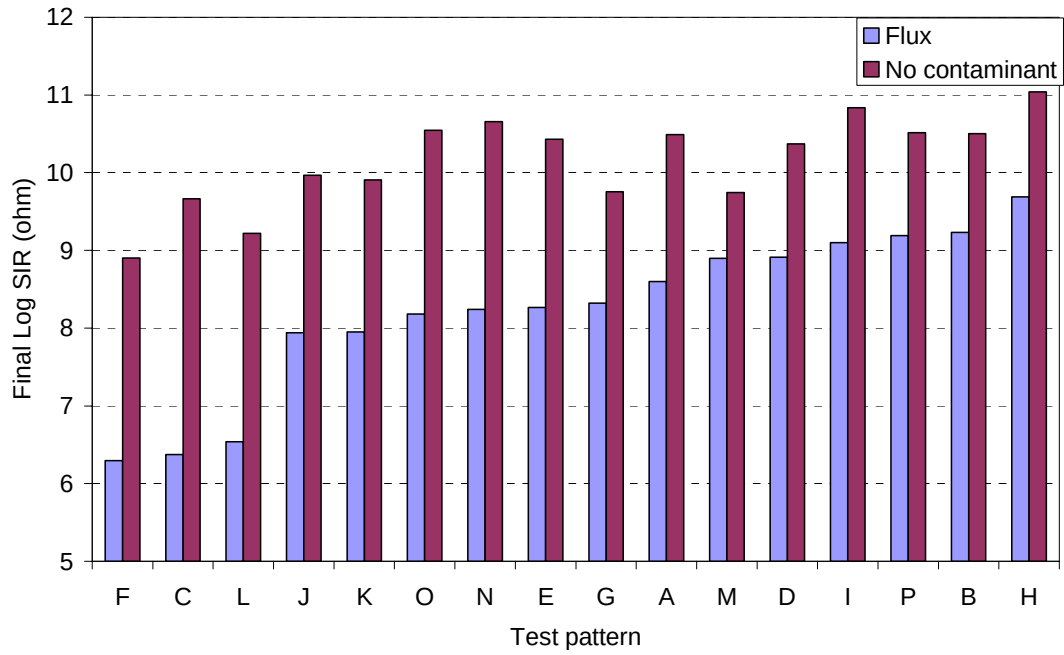


Figure A.25. Final SIR values for different test patterns with flux on the A assembly

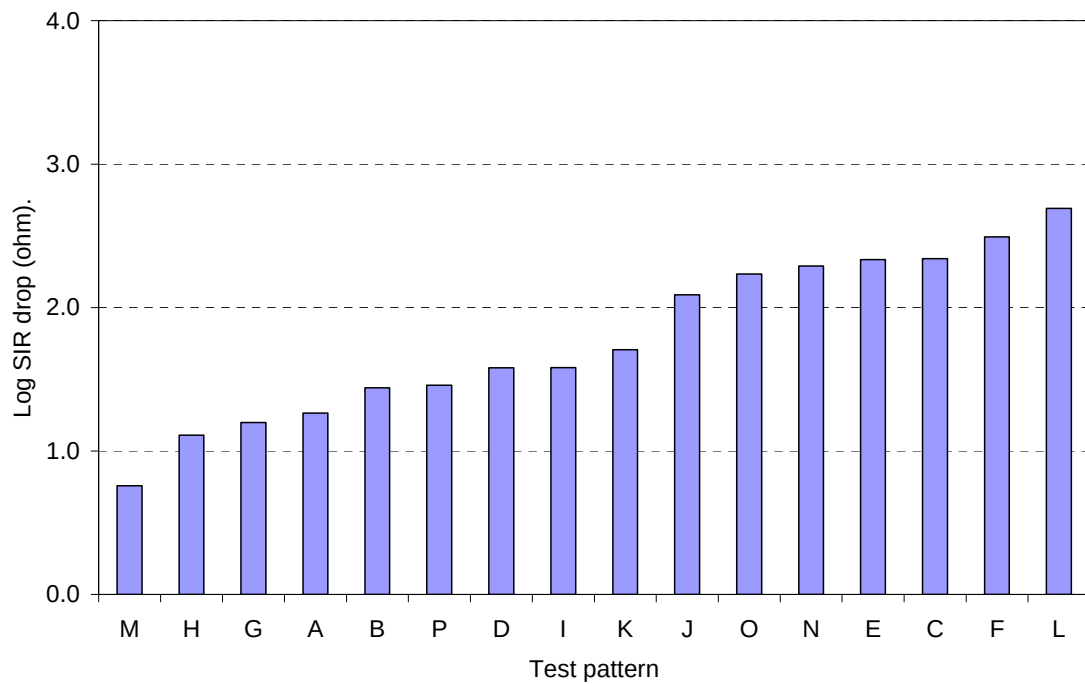


Figure A.26. Final SIR drop after flux contamination on the A assembly

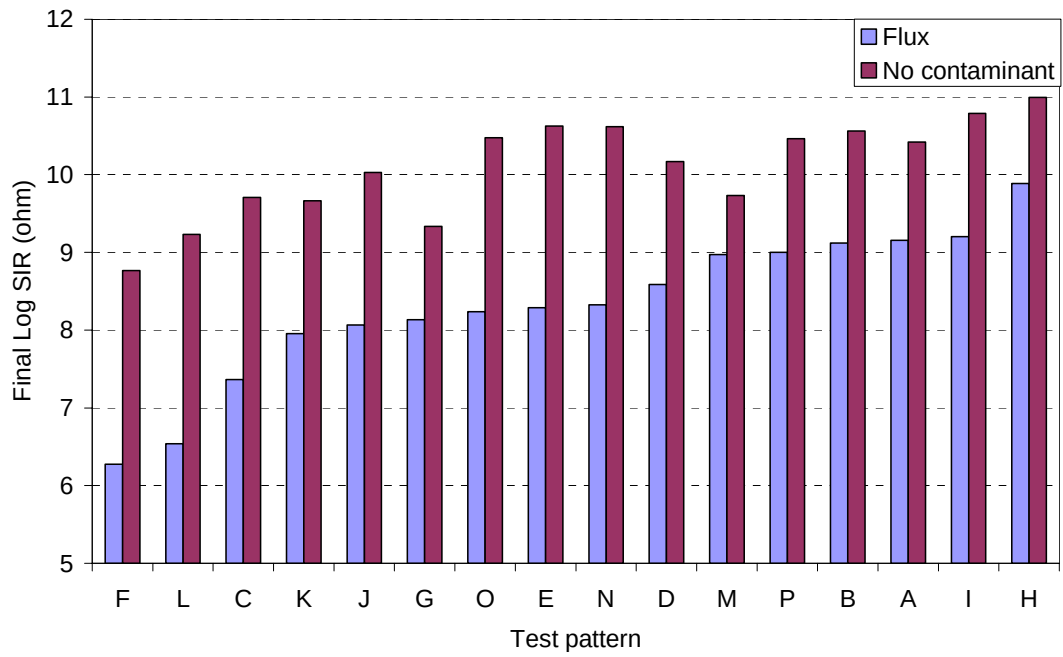


Figure A.27. Final SIR values for different test patterns with flux on the B assembly

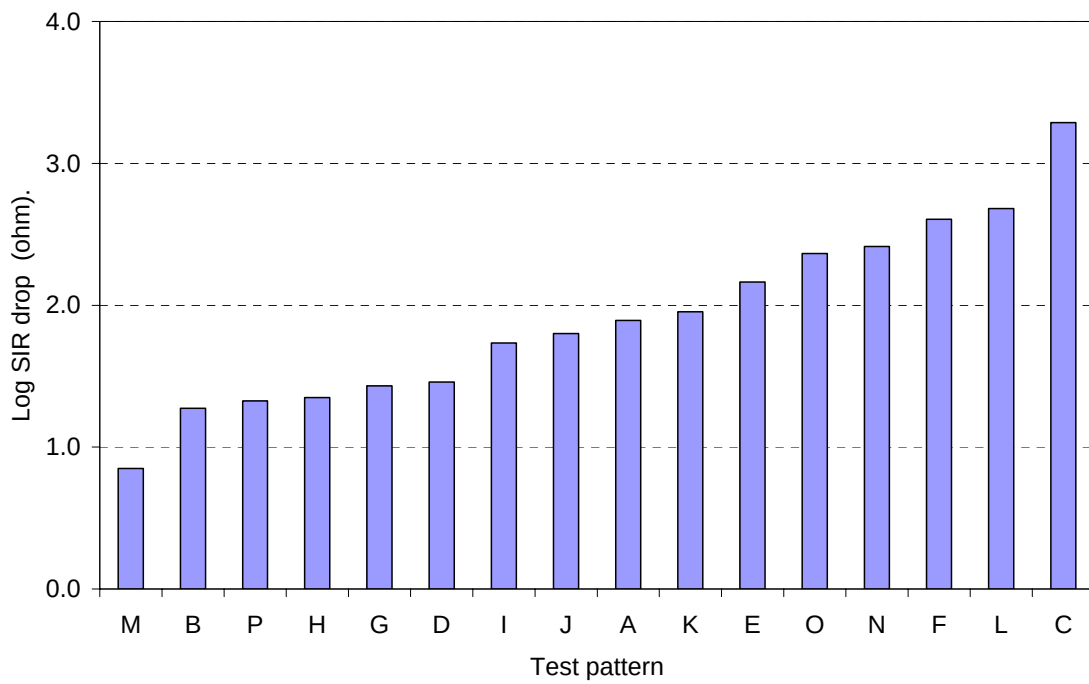


Figure A.28. Final SIR drop after flux contamination on the B assembly

These results clearly show that there is a dependence on the SIR patterns, and there were several factors that may influence the SIR results:

- **Coating coverage:** There were big SIR drops for BGA (test pattern C) and QFP components (test patterns: F and L) with flux contamination. This was probably because not all the coatings fully penetrated the underside of the BGA, as has been shown previously². The low SIR results from the QFP components can be attributed to a thinner coating on the sharp edge of the leads, as shown in Figure A.2. The same significant SIR drop was not seen on the SOIC leads components, this was probably due to the larger big solder pads and a side solder fillet on the SOIC components, enabling the coating to better cover the lead, as shown in Figure A.29. Consequently there was improved coating protection performance with the SOICs. A thinner coating on sharp edge of lead component does not always cause a coating protection problem, since the contaminants will adhere less on the sharp edge, similarly to the coating. The same trends were not found for the surfactant, and may be because of the stronger test condition of 85°C/85%RH reduced the SIR results to the lowest SIR value that can be measured by the equipment, i.e. 10^6 ohm.
- **Contaminant wettability:** The smallest drop in SIR was observed with the two comb patterns (K and G) underneath the QFP, when applying surfactant which suggests that the contaminant does not spread under the QFP. For the flux contaminant the SIR drop on comb pattern (K) underneath the coarser QFP, suggesting a higher wettability of the flux.
- **Contaminant distribution:** The same volume of contaminant was applied to similar areas for the different components type, but for high surface energy coatings (e.g. fluoroacylate coating) or low spreadability contaminant (e.g. surfactant in DI water), the contaminant did not cover the contamination area uniformly when the contaminant was applied to the defined contamination area. Figure A.30 shows an example for the surfactant contamination on chip capacitor test pattern (O). The actual contamination area, as shown in the white dots in the figure, was much smaller than the defined contamination area. The ratio of actual contamination area and defined contamination area varied on different component type. This makes the contaminant concentration variable on different test patterns. This can explain the big SIR drop on chip capacitor test patterns (O, N and E), where the actual contamination areas were much smaller than the defined contamination area compared with other components.
- **Component pitch:** Typically with fine pitch components there will be more flux residues from the assembly process, which can contribute to low SIR results. The test patterns, F, L and C, that have big SIR drop, all have low SIR values without contamination.

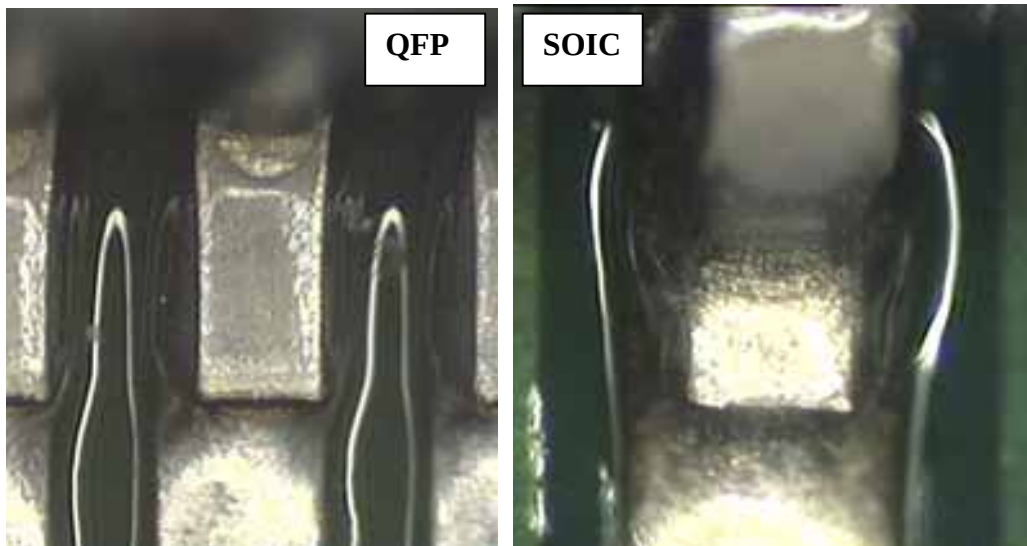


Figure A.29. Solder joints for QFP and SOIC components.

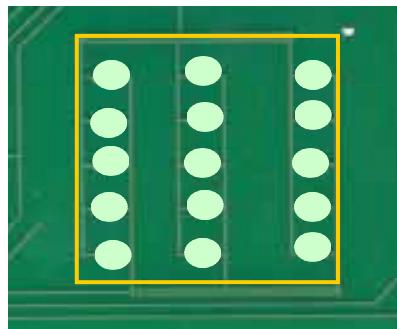


Figure A.30. Actual contaminant area on test pattern O

It is important to note there was not a single cause for low SIR values. All these influences make the comparison on SIR between patterns become more complex. However, this complication reflects the real situation of component contamination when assemblies are exposed to harsh environment. Therefore the test board does need to be as close to the real circuit in design and process. The current approach and test design have been shown to be powerful in identifying coating protection problems.

A.6.4 Visual inspection of coated PCBs after exposure SO_2

The coated PCBs were all inspected after each of four cycles of SO_2 exposure under a microscope. Significant differences in the level of corrosion were observed, that was dependent on the coating. The ranking following four exposure cycles from least to most corroded for SO_2 contamination is presented in Figure A.31. This visual inspection ranking did not agree well with the SIR drop measurements from these boards, as shown in Figure A.20. Solvent-based acrylic and water-based acrylic coatings showed

minor corrosion defects, but the SIR drop after exposure was significant. Hence visual inspection results can be useful in discriminating between the corrosion protection of coatings, if the corrosion products are not ionic and mobile, they will not influence the SIR results. Of course if corrosion process and resultant products bridge or reduce insulated substrate gap the SIR values will drop. Therefore, it is important to acknowledge that it is the SIR results that reflect circuit reliability. However corrosion of some structures are more sensitive, such as thin metal tracks where corrosion may cause an open circuit.

Ideally the SIR measurement shall be performed during SO₂ exposure, but this is very difficult due to corrosion of cabling inside the SO₂ chamber. Following exposure the boards should be SIR tested as soon as possible, less than 2 hours, since SO₂ will diffuse out of the coating. However, for these boards the SIR measurement were taken after a few days following exposure, hence SIR results did not correlate well with the visual inspection results.

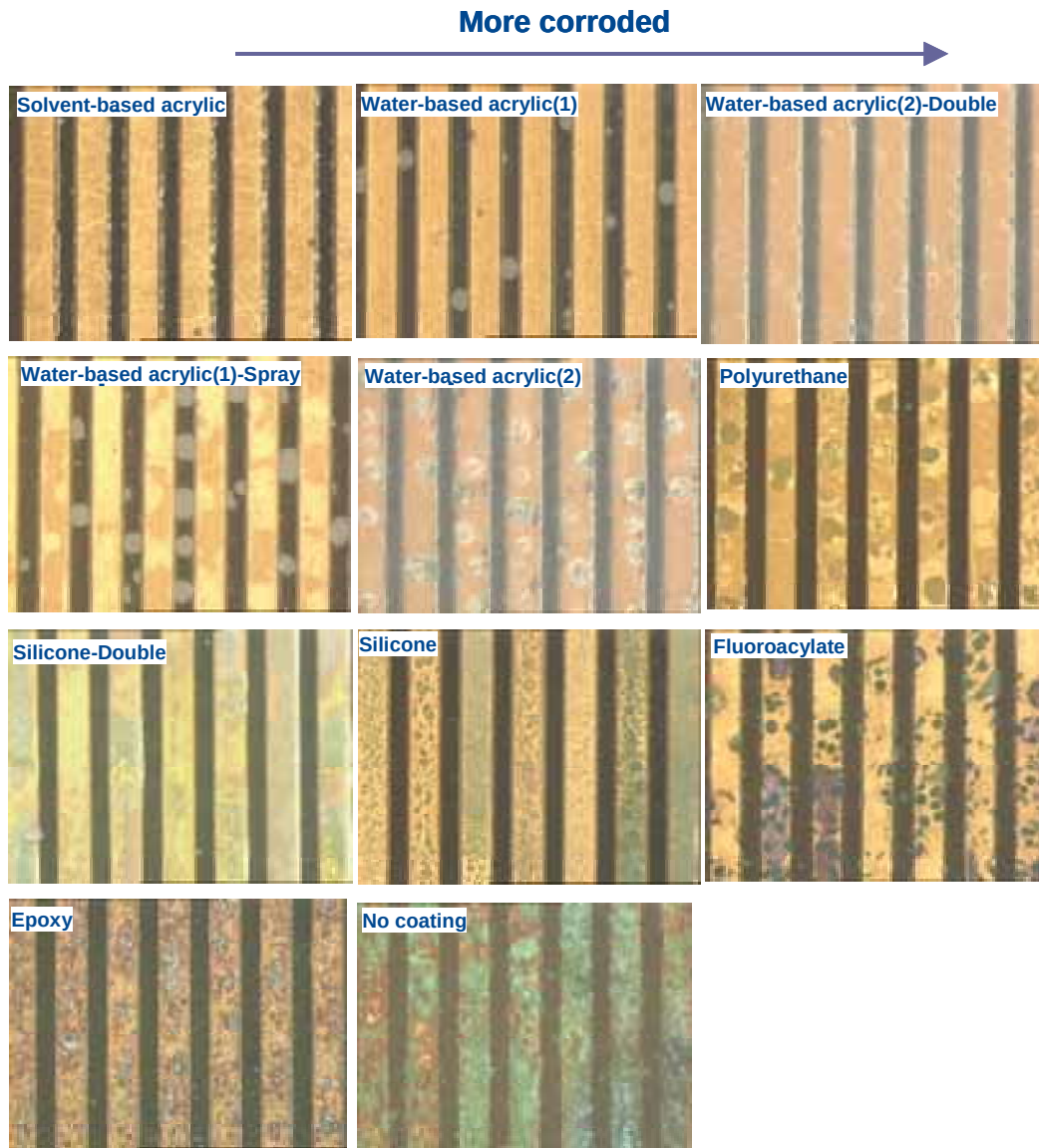


Figure A.31. Corrosion appearance on coated TB67 PCBs after SO₂ exposure

A.6.5 Effect of flux residues on coating protection performance

The results in previous section (Figure A.5) have indicated that the assembly process from two manufactures left some flux residues which decreased the SIR result, particularly for the test patterns with fine pitch components on uncoated assembly. Here the average final SIR values on assembly A and B from all the test boards and different coatings before and after contamination is plotted in Figure A.32. It is evident from this figure that the SIR difference between assembly A and B before contaminating remained the same after contaminating for most patterns. This indicates the importance of board cleanliness in maintaining coating protection performance. Conformal coatings do not protect boards with contamination underneath the coating.

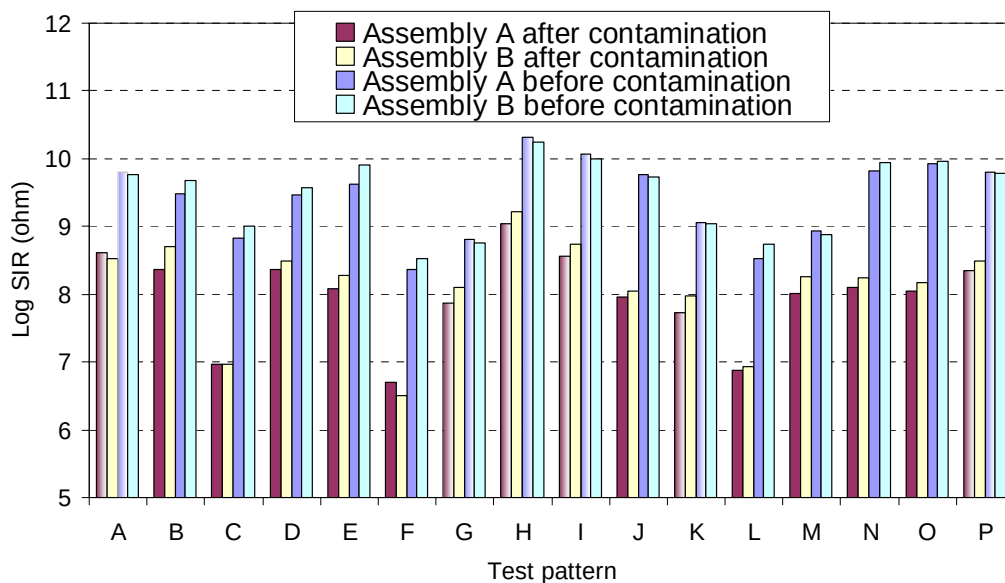


Figure A.32. Final SIR for A assemblies and B assemblies before and after contamination

A.7 CONCLUSIONS

The experimental results presented here, have used the new test method and recommended test parameters and with the new test assembly design, and has been successful in characterising the conformal coating protection performance in harsh environments. The combination of final SIR and SIR drop results provides an indication of the permeability of the coatings to moisture and contaminants from environments.

Coating protection performance is dependent on coating chemistry, coverage and contaminants. Therefore, when assessing coating protection performance, the contaminants should be selected to represent the harsh environment in which the electronic assembly will be used. Using a contaminant solution to contaminate test assembly is a feasible method to simulate an assembly exposed to a harsh environment.

The test conditions are significant and to achieve the optimum discrimination it is recommended is to use the following test conditions of 40°C/93%RH with 5V bias test for contaminated assembly, and 40°C/93%RH with 50V bias test for uncontaminated assembly. The 85°C/85%RH test condition is too strong for measuring contaminated boards, and the SIR results are more dominated by water permeability of the coating.

The new test board assembled with a wide range of components has shown advantages in identifying conformal coating protection problems on specific components. There is potential protection failure on fine pitch leads components and BGA components, where coating coverage is a particular issue.

Visual inspection of coated PCBs after SO₂ exposure showed a reasonable good degree of correlation with the SIR results. This method can be used to determine coating corrosion protection performance from industry pollution gas. However, it should be emphasised that only the SIR technique is capable of providing information on the reliability of the underlying circuit.