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**Effect of Voiding on
Lead-Free Reliability**

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Effect of Voiding on Lead-Free Reliability

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ABSTRACT

As a result of this work, in which seven different solder pastes from three manufacturers have been evaluated through a range of reflow profiles, end-users can have a high degree of confidence that voiding levels in lead-free solder pastes can be kept below the IPC specified maximum of 25% by area. No paste exhibited voids in any PBGA joint greater than 15% despite attempts to produce higher voiding levels.

Three different voiding levels were produced and samples subsequently subjected to 2000 thermal cycles (-55 to +125°C). Despite these samples having higher voiding levels than those stipulated for class 3 of the IPC's BGA Assembly and Inspection Guidelines, no adverse effect on reliability was seen. The shear strength deterioration during thermal cycling of chip resistors also with these levels of voiding, was also unaffected.

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1 INTRODUCTION

European legislation will eliminate lead in solders from main-stream electronics manufacture, by 1st July 2006. The current preferred solder replacements are based on the tin-silver-copper (SAC) system, which have melting points of 217 °C and above. This 34 °C increase in melting point from the established SnPb solder alloys, necessitates a similar increase in processing temperature for both reflow and wave soldering. Some users have reported increased voiding levels associated with these higher temperatures (Reference 1) and this has led to a general belief within the electronics industry, that the change to lead-free soldering will mean an increase in typical voiding levels and potential consequential reductions in solder joint reliability.

For SnPb alloys, a good deal of work on assessing reliability of soldered joints with known voiding levels has been undertaken. Voiding has been shown to reduce solder joint reliability in a number of ways. Large voids cause reductions in effective cross-sectional area of the soldered joint (Reference 2). This results in higher joint stresses as any shear strain on a void-containing joint is experienced over the reduced cross-sectional area. The voiding may also reduce the distance fatigue cracks have to propagate to cause failure, although alternatively, voids may act as crack arrestors, stopping the propagation of a crack and requiring additional energy to initiate a continuing crack through the remainder of the joint (References 3 and 4).

The effect on reliability of smaller voids is more complicated and can depend on where the voids are located within the joint. The latest IPC BGA assembly guidelines (Reference 5) specifically differentiate between voiding within the bulk of the joint and voids at the interface between component and solder, or between solder and PCB. Voids at the interfaces tend to be more detrimental and have therefore been given a lower permitted level in these guidelines than voids in the bulk of the joint.

Voids have been shown to have a direct effect on reliability, with several workers (References 4 and 6) reporting premature thermal cycling failures and significant loss of electrical integrity, as well as device failure due to voiding. The device failure may be related to loss of device thermal performance due to voiding, which can result in device over-heating and subsequent premature performance failure.

Smaller voids in the bulk solder of the joint may have less effect on reliability. Banks et al (Reference 3) have reported no reduction in the reliability of plastic ball grid arrays (PBGA) with up to 24% voiding by area. Indeed, their work showed an improvement in PBGA reliability with voiding levels up to 16%. In these samples the route taken by cracks within the solder balls, was not affected by the presence of voids. Banks et al suggested several possible reasons for this improved reliability. As discussed above, the voids may be acting as crack arrestors. The inclusion of voids within the joint does increase the height of the solder joints (possibly by as much as 4%). This will reduce the stress on a taller joint for the same joint strain, compared to a shorter joint. It may simply be that the mechanical properties of the joint are affected by the inclusion of the voids, making the structure more flexible. The improved reliability of joints with limited voiding levels is probably a result of a combination of some or all of these three suggestions.

The belief that voiding is likely to be greater for lead-free solders is consistent with many of the known causes of voiding, for example solvent retention within the molten solder of the joint can cause voiding. This may be more likely in lead-free soldering, as there may be insufficient preheat in a poorly developed profile, which is particularly likely to occur during initial transition to lead-free soldering. Lead-free solders have higher surface tensions (Reference 8) than SnPb equivalents, which may also result in to increased solvent retention. Air Liquide (Reference 9) have reported that increased oxidation at the surface of joints can inhibit out-gassing of volatile molecules. Such increased surface oxidation is likely to occur with the higher processing temperatures of lead-free soldering. Lea reported increased voiding in SnPbAg solder joints (Reference 10) where the solder paste had experienced increased oxidation during the assembly process. Again, the increased processing temperatures of lead-free soldering are consistent with this scenario.

At the higher lead-free processing temperatures, increased out-gassing of the component parts may occur, leading to increased voiding in the joints. Out-gassing may be caused by insufficient laminate or solder mask cure (Reference 2). Moisture absorption or surface contamination may also increase voiding in the soldered joint. Several workers have reported problems with vias within pads (References 11 and 12), an increasingly common aspect of high density PCB designs. Such vias may be more prone to out-gassing at higher processing temperatures.

Eckel et al (Reference 4) have also reported that increased processing temperatures may affect the out-gassing of electroless nickel/immersion gold (ENIG) surface finishes. The out-gassing may be caused by organic contaminants within the gold finish, with hot air solder levelled (HASL) finishes performing better. Similar issues may exist with organic solderability preservative (OSP) on copper finishes.

The vast majority of the work cited above, has been conducted on SnPb systems. But the results clearly provide a link between voiding, soldering and reliability of the joint. In consequence, it is reasonable to question the nature and extent of any link between voiding and reliability for lead-free soldered joints. However, there is very little work in the open literature concerning lead-free systems. Thus the work reported here was designed to investigate some of these issues for lead-free systems, specifically for the SnAgCu alloy.

2 TEST ASSEMBLY DESIGN, MANUFACTURE AND TESTING

2.1 EXPERIMENTAL PHILOSOPHY

The work in this study was carried out in two phases. The same test assembly design was used for both phases. Phase 1 utilised a range of reflow profiles in order to determine three suitable sets of process parameters generating three different voiding levels. Phase 2 utilised these three sets of parameters to manufacture three series of assemblies, which were subsequently thermally cycled. These assemblies were then monitored for continuity failure and shear strength deterioration.

2.2 COMPONENT SELECTION

When field failures occur in solder joints, these are generally associated with components that have a large thermal coefficient of expansion (TCE) mismatch with the substrate on which they are mounted. Therefore, this work concentrates on failures and failure modes within these component types, since these were the structures most likely to fail first in a field environment.

This work utilised three component types; ceramic chip resistors, small outline ICs (SOICs) and PBGAs. Chip resistor components are present in most electronic assemblies. Due to their alumina bodies, they have a TCE much lower than common substrate materials. Because of this and having no compliant leads, these components are more prone to fail from cyclic strain damage accumulating in the joints than other component types. This scenario is shown schematically in Figure 1. The magnitude of the effect is dependent on the component size. Two resistor sizes have been utilised in this work, R1206 and R0603. R0603 resistors are the commonest size utilised in electronics design today. R1206 resistors are larger and have been included to give earlier indications of failures.

Being generally cuboid in shape with vertical sides, these components lend themselves to shear testing, and which can therefore be used as a measurement method of cyclic fatigue. In these experiments only pure tin plated components were used.

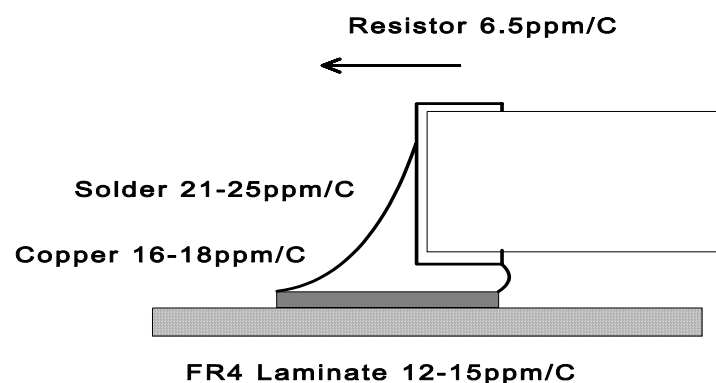


Figure 1: Schematic cross-section of a SM assembly highlighting the CTE (X-axis) mismatches.

The second type of component utilised were SOICs. These represent gull wing lead devices, and are very common in current SM designs. The compliant leads usually give lower strain levels than for leadless ceramic components, but the components were included to ensure that no unpredicted failure modes occurred with lead-free gull-wing joints. The surface finish of these components was again tin.

The final type of component used were PBGAs with SAC balls. Although these components have a BT-epoxy laminate, their TCE is constrained in the region of the silicon die, which can lead to early thermal cycling failures.

2.3 PCB DESIGN

The vehicle design used is shown in Figure 2. The components incorporated are listed in Table 1. The square section in the top left hand corner of the test board was specially designed for easy detachment and was utilised for shear testing. The lower left portion of the design was not utilised in these trials. The remainder of the components were interconnected via daisy chains to the edge connector on the right hand side of the design, for easy monitoring of electrical continuity. The PCBs were each fabricated as a 6-layer FR4 multilayer of thickness 1.6 mm. Cu thickness was 35 μm (Cu plating 1 oz/sq.ft) and the surface finish was immersion gold over electroless nickel (ENIG). This finish was used as it is lead-free, in common usage, and widely available from most PCB manufacturers.

Table 1: List of components mounted on the test substrate

Component	Number of components mounted on a substrate
R1206	40
R0603	40
SOIC14	6
PBGA256	2

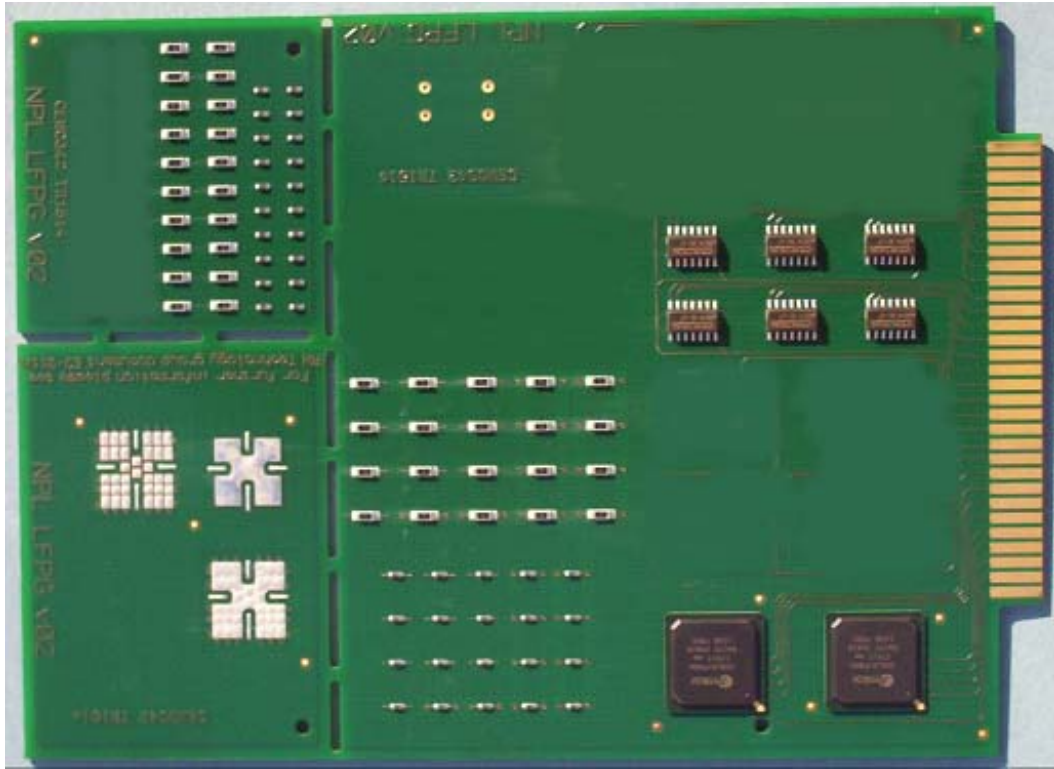


Figure 2: Test board layout (81 × 65 × 1.6 mm)

2.4 PCB ASSEMBLY REFLOW PROFILES

Substrates were stencil printed with solder paste using a stainless steel stencil with a thickness of 150 μm (0.006"). The pastes used were all 95.5Sn3.8Ag0.7Cu alloy. Components were placed onto the substrates using automatic and semi-automatic (for PBGA) placement systems. These processes ensured a consistent solder joint volume.

Reflow of lead-free solder paste was achieved using three different profiles (see **Table 2**). The soldering profiles were measured at 5 different locations on a fully populated test assembly. The resultant profiles represent a typical lead-free profile (profile 1) with two additional profiles having faster ramps, which it was hoped would increase the solvent retention in the pastes.

Table 2: Reflow temperature profile details

Thermocouple position	Profile 1			Profile 2			Profile 3		
	Max Temp °C	Time above 217°C	Time to Max Temp (min)	Max Temp °C	Time above 217 (min)	Time to Max Temp (min)	Max Temp °C	Time above 217°C	Time to Max Temp (min)
PBGA Inner	245	00:54	03:24	240	00:45	03:17	249	00:57	02:45
PBGA Outer	239.5	00:47	03:29	234	00:36	03:13	243	00:47	02:43
SOIC	241.5	00:43	03:25	231.5	00:29	03:06	243	00:44	02:35
R0603	253.5	00:50	03:14	251	00:44	02:59	259	01:03	02:30
R1206	233.5	00:39	03:22	225	00:22	03:06	238	00:34	02:38

2.5 SOLDER PASTES

Seven solder pastes were used in this work, from 3 different suppliers, as detailed in **Table 3**. Six of the pastes were based on no-clean flux technology, whilst the seventh was a water soluble paste. In addition to being processed through different profiles, pastes A and B were also processed on PCBs which had been aged by passing them through a lead-free reflow profile (2 or 4 times) prior to assembly. Some samples of PCBs printed with paste H were also subjected to 4 hours in a damp heat chamber at 40 °C/93%RH, to encourage the paste and PCB to take-up moisture prior to reflow.

Table 3: Lead-free solder paste details

Paste	Manufacturer	Alloy	Flux Type	Particle Size	Metal Content wt%
A	X	95.5Sn3.5Ag0.7Cu	No-clean A	Type 3	88.5
B	X	95.5Sn3.5Ag0.7Cu	No-clean A	Type 3	88.0
C	X	95.5Sn3.5Ag0.7Cu	No-clean B	Type 3	88.5
D	X	95.5Sn3.5Ag0.7Cu	No-clean C	Type 3	88.5
F	Y	95.5Sn3.8Ag0.7Cu	No-clean E	Type 3	89.8
G	Z	95.5Sn4.0Ag0.5Cu	No-clean F	Type 3	88.0
H	X	95.5Sn3.5Ag0.7Cu	Water-Soluble	Type 3	88.5

2.6 BUILD QUANTITIES

For each of the combinations of solder reflow profile and solder paste tested in phase 1, two assemblies of each combination were manufactured. Of the three combinations of reflow profile and solder pastes chosen for phase 2, ten assemblies of each combination were manufactured.

2.7 X-RAY INSPECTION

After assembly, voiding levels were measured using Dage XIDAT 6000 X-ray system. The system was set up with identical parameters for each inspection run so that the results obtained are directly comparable. For the BGAs, an auto inspection routine was utilised, which calculates the total area of voids in each PBGA solder joint. Figure 3 presents a typical image. Representative images were also acquired of resistors and SOICs for each condition.

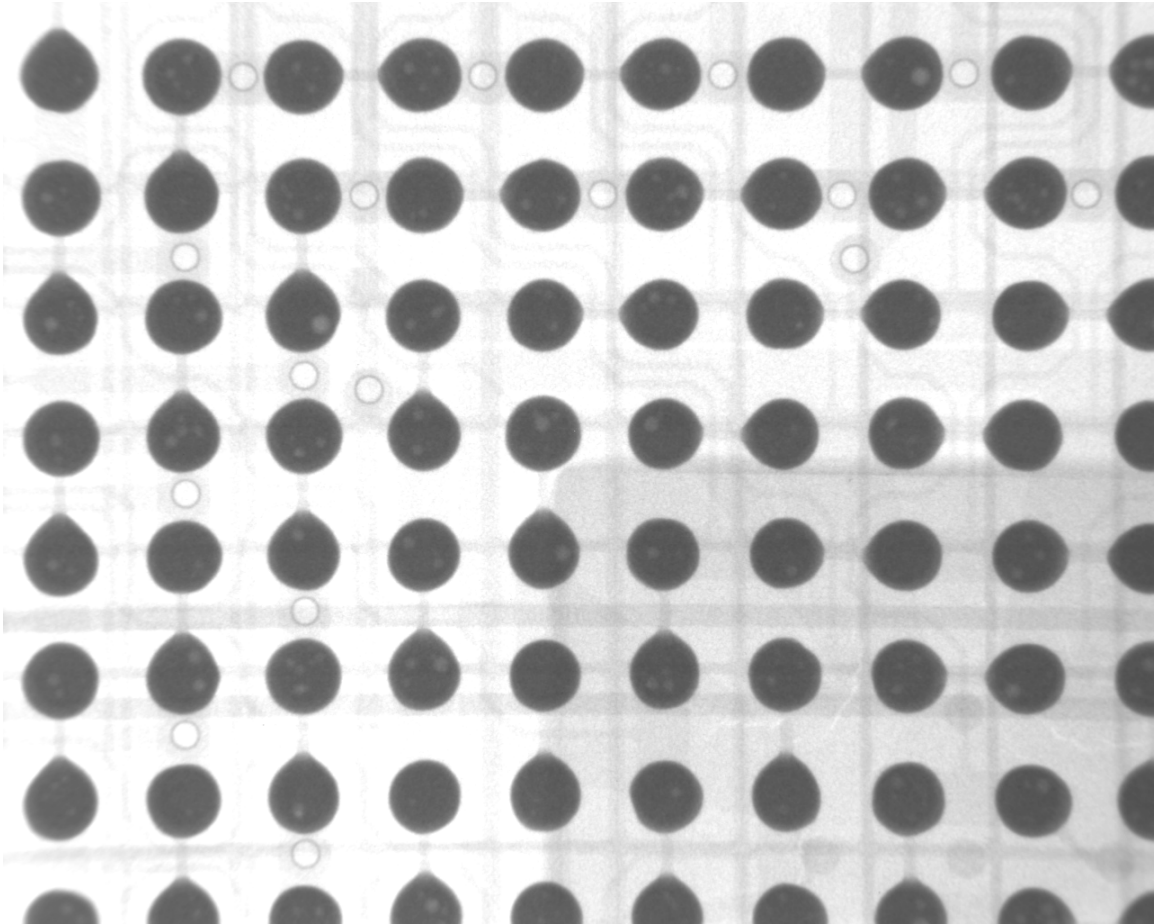


Figure 3: Example of BGA X-ray image

2.8 VISUAL INSPECTION

After soldering, all the non-BGA joints on the assemblies were 100% visually inspected by a single operator using a 10X to 30X stereo microscope. The assemblies were inspected to IPC A610 Rev C class 3 (Reference 13). No rework was undertaken. Any defective solder joints were logged and removed from subsequent test results.

2.9 THERMAL CYCLING AND ELECTRICAL TEST

The thermal profile used to condition the samples was -55 to +125°C with 5min dwells and a ramp between dwells of 10 °C/min, and is shown in Figure 4. Temperatures were measured at four points on a populated assembly: on solder joints of R0603, R1206, SOIC joints and a PBGA joint. All measured points were within a few degrees of each other throughout the thermal cycle.

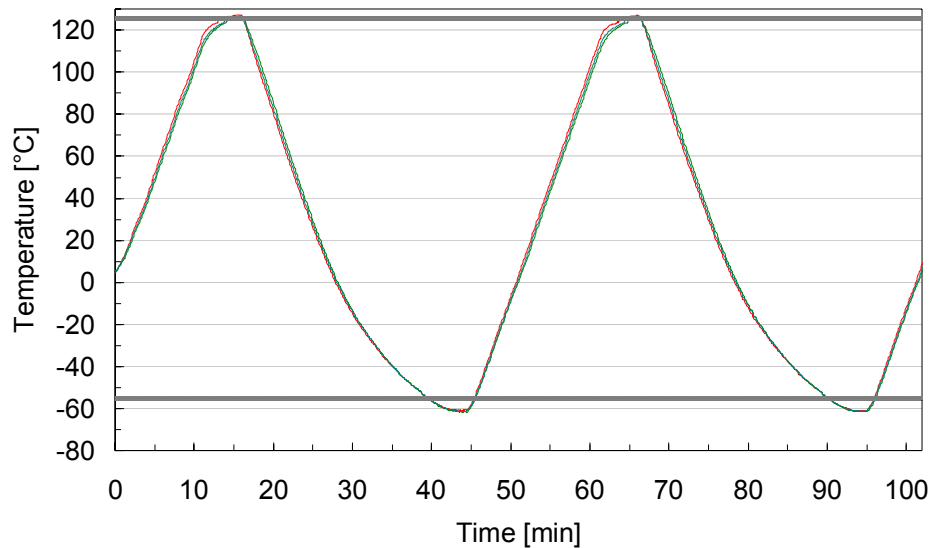


Figure 4: Thermal cycling profile (-55 to 125°C, 5min dwells, ramp 10°C/min)

For phase 2, one assembly from each batch of the manufactured test vehicles was removed after each of 0, 500, 1000, 1500 and 2000 thermal cycles. These assemblies were subjected to shear testing and micro-sectioning. Five assemblies from each batch were subjected to the full 2000 thermal cycles with periodic electrical measurement using an automatic switching system and digital ohmmeter at 0, 500, 1000, 1250, 1500, 1750 and 2000 cycles.

2.10 SHEAR TESTING

The chip resistors are well suited to shear testing, having a flat edge for the chisel tool to address. Shear testing of resistors is illustrated in **Figure 5**.

The R1206 and R0603 components were tested on the board in order to determine the ultimate shear strength for the joints (the maximum force prior to fracture).

For the shear tests the stand-off height of the chisel tool above the PCB surface was 80 µm. During each test, the shear tool was moved forward at a defined speed of 200 µm/s against the test component, and the force was monitored until the solder joint broke. The shear tester used was a Dage Series 4000, with a DS 100 Kg testing head. Twelve R0603 and R1206 chip resistors were tested for each condition (24 on each PCB). All shear testing was undertaken at room temperature.

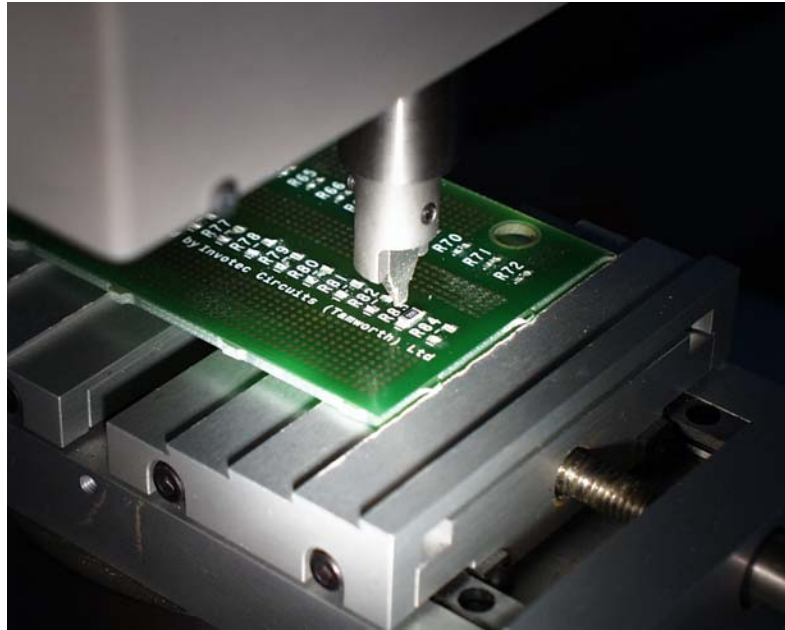


Figure 5: Shear test jig and push-off tool

2.11 MICRO-SECTIONING

After thermal cycling, samples were cut from test boards in such a way as to minimise stress using a diamond saw. This method of cutting ensures that soldered joints are not overheated or stressed to levels that might affect joint microstructure. For the same reason cold curing epoxy resin was chosen as the most suitable mounting compound. Samples were ground with successive grades of silicon carbide grit papers, followed by polishing with diamond pastes/sprays with successively smaller particle sizes. The micro-sections were inspected using a scanning electron microscope in backscatter mode. This process enabled easy location of cracks within the samples.

3 RESULTS

3.1 PHASE 1 PASTE EVALUATION

The voiding levels in the solder joints from the measurement on the various assembly trials are given in Table 4. The average value is calculated as an average of 256 joints of 2 devices on 2 assemblies, i.e. an average of 1024 solder joints.

Table 4: Average voiding levels in phase 1 paste evaluation

Parameter Set	Paste Type	Profile Number	Pre-assembly Reflow Passes	Damp Conditioning	Average Voiding %	Maximum Void Size %
1	A	2	0	N	3.03	11.2
2	A	1	0	N	3.17	11.4
3	B	2	0	N	3.02	12.9
4	B	1	0	N	3.11	12.1
5	C	2	0	N	2.97	9.4
6	C	1	0	N	3.20	9.3
7	D	2	0	N	3.25	12
8	D	1	0	N	2.82	11.2
9	A	3	0	N	2.00	9.2
10	A	3	2	N	2.65	13.1
11	A	3	4	N	2.16	10.6
12	A	2	2	N	2.38	11.7
13	A	2	4	N	1.85	10.5
14	B	3	0	N	1.85	10.8
15	B	3	2	N	2.18	8.9
16	B	3	4	N	2.04	13.6
17	D	3	0	N	1.80	10.6
18	F	3	0	N	3.45	9.1
19	F	2	0	N	2.64	14.1
20	G	3	0	N	3.49	14.3
21	G	2	0	N	3.21	11.9
22	H	3	0	N	2.12	13.3
23	H	3	0	Y	2.64	14.49
24	H	2	0	N	1.77	10.5
25	H	2	0	Y	2.80	12.5

From the above assembly trials, the three parameter sets 2, 9 and 20, giving a range of voiding levels, were chosen for the phase 2 trials, and were designated sets M, L and H respectively.

3.2 PHASE 2 VOIDING LEVELS

The voiding levels in the PBGA solder joints from the various assembly trials are given in Table 5. The average value is calculated as an average of 256 joints of 2 devices on 10 assemblies, i.e. an average of 5120 solder joints. These voiding levels differ slightly from the phase 1 results, because the X-ray system set-up differed and the average was generated over a greater number of joints.

Table 5: Average voiding levels in Phase 2 paste evaluation

Parameter Set	Phase 2 Designator	Maximum Void Size %	Average Voiding %
9	L	9.68	0.9
2	M	9.53	1.5
20	H	13	3.1

3.3 THERMAL CYCLE ELECTRICAL TEST RESULTS

3.3.1 R0603 Electrical Test Results

Percentage failures for R0603 components are given in Table 6 and with the failure development presented graphically in Figure 6. The failure criterion was set at 200Ω , 100Ω greater than the resistor value. Due to the circuit design, it was not possible to determine whether the failures detailed below occurred in the soldered joints of the component or in the associated via linking the component to the edge connector used for electrical test.

Table 6: R0603 electrical test results

Number of cycles	H	M	L
0	0%	0%	0%
500	0%	0%	10%
1000	0%	14%	20%
1200	0%	18%	24%
1400	0%	22%	24%
1600	0%	22%	24%
1800	4%	24%	30%
2000	4%	26%	30%

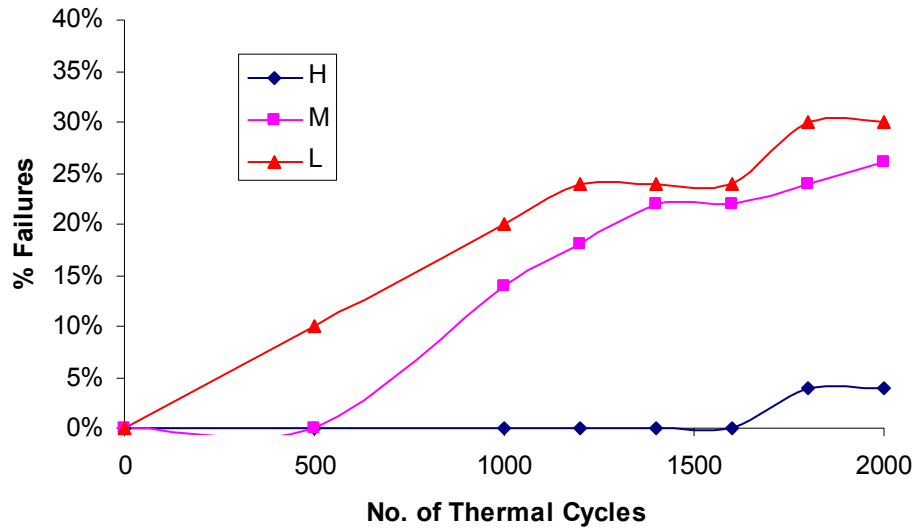


Figure 6: R0603 electrical test failures

3.3.2 R1206 Electrical Test Results

Percentage failures for R1206 components are given in Table 7 and with the failure development shown graphically in Figure 7. The failure criterion was set at 1100Ω , 100Ω greater than the resistor value. The data were corrected for any failures that occurred in the vias and tracking associated with the electrical test circuit.

Table 7: R1206 Electrical Test Results

Number of cycles	H	M	L
0	0%	0%	0%
500	2%	0%	0%
1000	10%	2%	12%
1200	12%	10%	16%
1400	14%	16%	20%
1600	14%	24%	28%
1800	16%	26%	28%
2000	18%	28%	32%

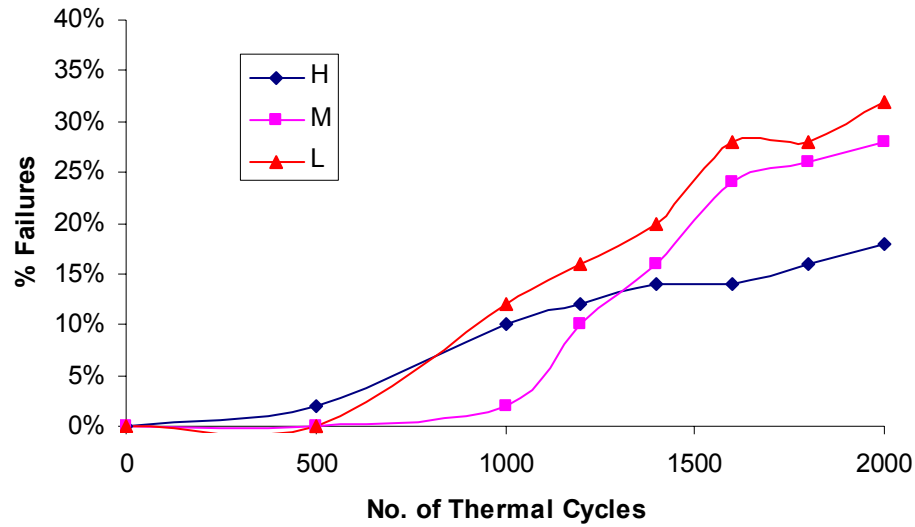


Figure 7: R1206 electrical test failures

3.3.3 SOIC Electrical Test Results

No electrical test failures occurred with the SOIC components during 2000 thermal cycles. The failure criterion was set at 100Ω for each component daisy-chain.

3.3.4 PBGA Electrical Test Results

All the failures that occurred in the PBGA components occurred in the C-ring, closest to the edge of the die in the component (see **Figure 8**). Percentage failures are given in **Table 8**, with the failure development presented graphically in **Figure 9**. The failure criterion was set at 100Ω for each daisy-chain of joints (four per component).

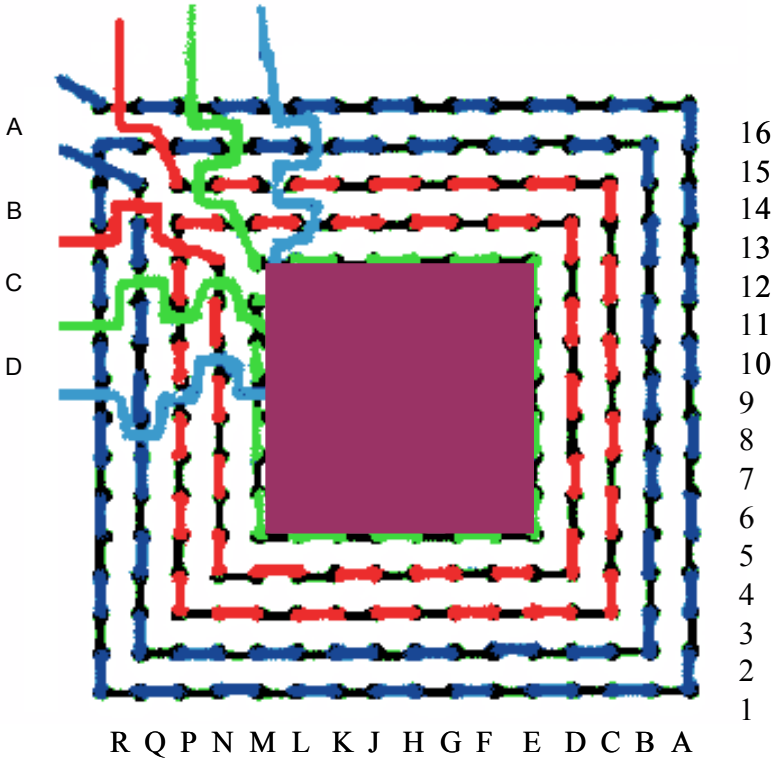


Figure 8: Interconnection circuits on PBGA components

Table 8: PBGA electrical test results

Number of cycles	H	M	L
0	0%	0%	0%
500	0%	0%	0%
1000	0%	0%	0%
1200	0%	0%	0%
1400	0%	0%	0%
1600	3%	0%	3%
1800	5%	0%	3%
2000	8%	5%	5%

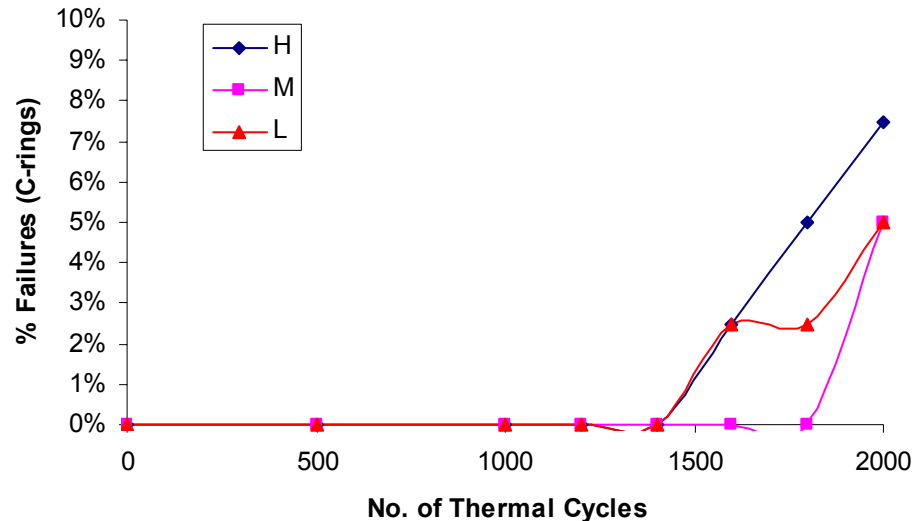


Figure 9: PBGA Electrical Test Failures

3.4 PHASE 2 SHEAR TEST RESULTS

Figure 10 shows the shear force required to remove the R0603 components. Figure 11 presents similar results for the R1206 components. The data obtained in the test were analysed in terms of the ultimate shear force required to rupture the solder joint, and then plotted as a function of the number of thermal cycles to which the assembly had been subjected. A mean value was calculated from the 12 individual measurements and plotted as a full dot, together with the first and third quartile of a box-whisker diagram.

The box-whisker diagrams reveal the distributions of ultimate shear forces measured after reaching a certain number of cycles. Although the testing was performed after a defined number of cycles, the locations of boxes plotted in the diagram have been moved sideways around the nominal number of cycles to avoid overlaying of data. The top and bottom sides of the boxes indicate first and third quartile (Q1, Q3) values of the population sample. The line drawn across a box is an indication of the median (quartile Q2). The vertical lines (whiskers) from these boxes extend to the last data point within the range of the limits. The upper and lower limits are calculated according to the relationships:

$$\text{Min. Lower Limit} = Q1 - 1.5 (Q3 - Q1), \quad \text{Max. Upper Limit} = Q3 + 1.5 (Q3 - Q1)$$

The full dot represents the population mean, and the asterisks (*) are outliers (data points above the fourth quartile or below the first quartile).

The data clearly show a reduction in shear strength as the thermal cycling progresses, due to the formation of fatigue cracks within the soldered joints of the chip resistors. *However, the data do not show any significant difference between the results for the different voiding levels in this study.*

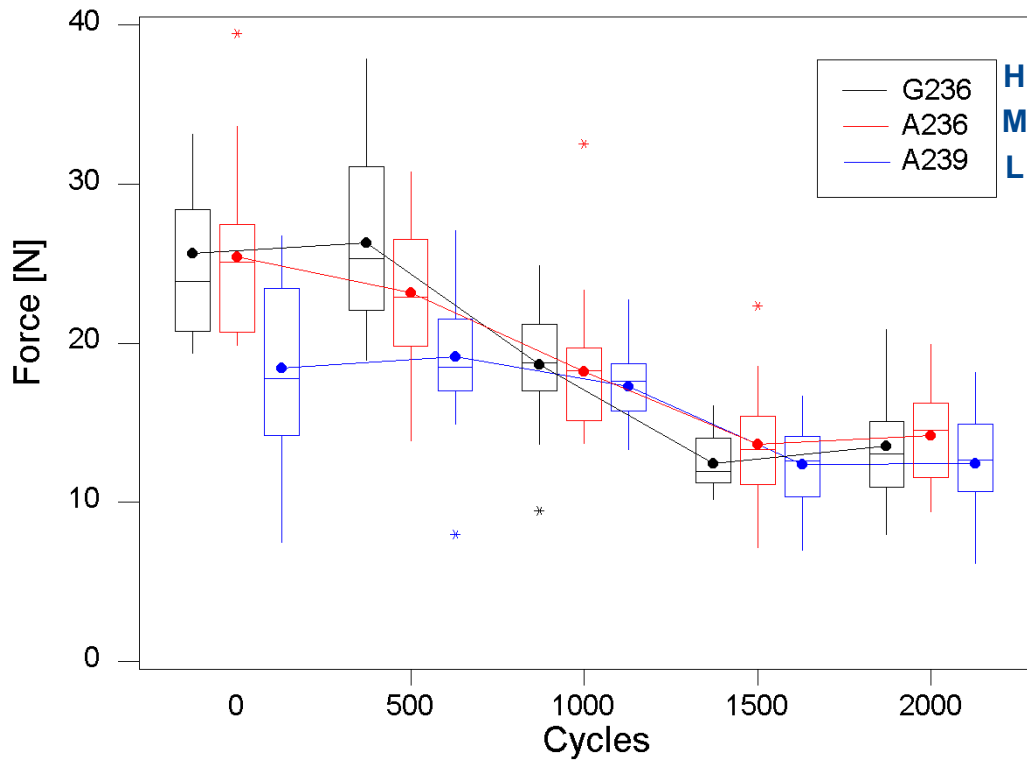


Figure 10: Shear test results for R0603 components over 2000 thermal cycles

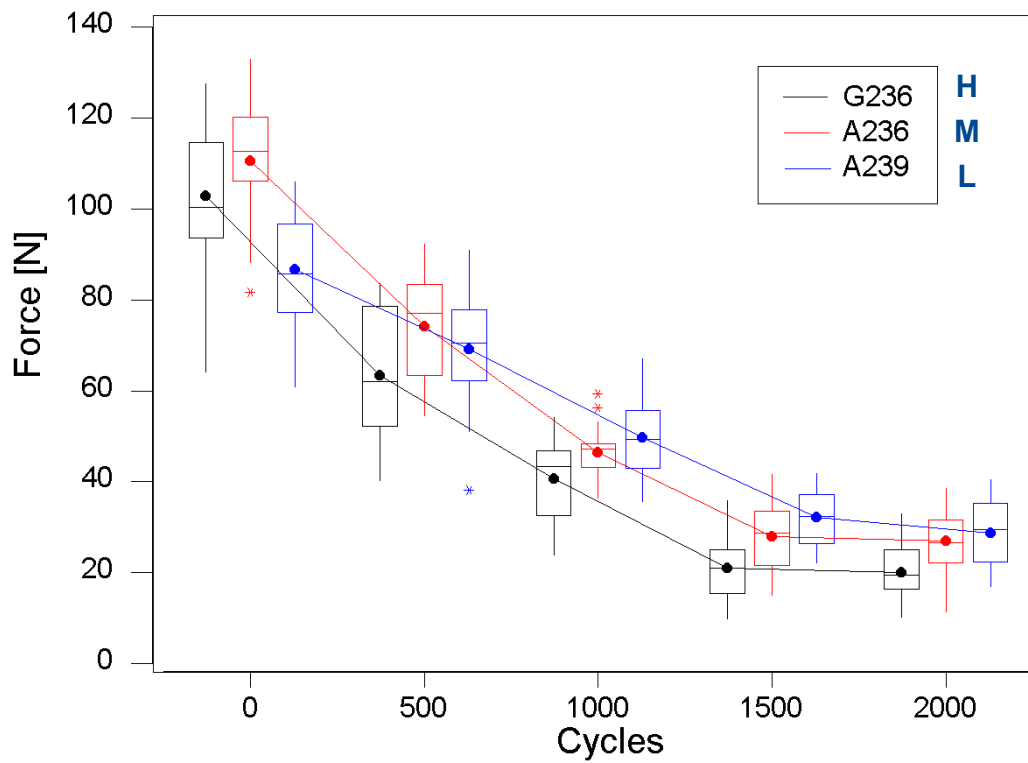


Figure 11: Shear test results for R1206 components over 2000 thermal cycles

4 DISCUSSION

4.1 PHASE 1 SOLDER PASTE TRIALS

The phase 1 solder paste trials were intended to identify three levels of voiding appropriate for the phase 2 evaluation, in which three sets of samples were to be assembled at these voiding levels. The desired voiding levels were intended to be very low (or zero) average voiding, moderate average voiding levels around 10%, and a high average voiding level around 20+%. However, from the results given above in section 03.1, it can be seen that generating these higher average voiding levels, above 5% proved impossible. Figure 12 shows the results for six different pastes from 3 different manufacturers using profile 3. All the pastes exhibited average voiding levels below 3.5%, with the largest voiding in any ball varying between 9 and 15%. Although pastes F and G exhibited slightly higher average voiding levels, these were not significantly different from the other pastes. Paste H was the water-soluble paste. All of these voiding levels are well below the 25% maximum voiding level specified by IPC (Reference 13).

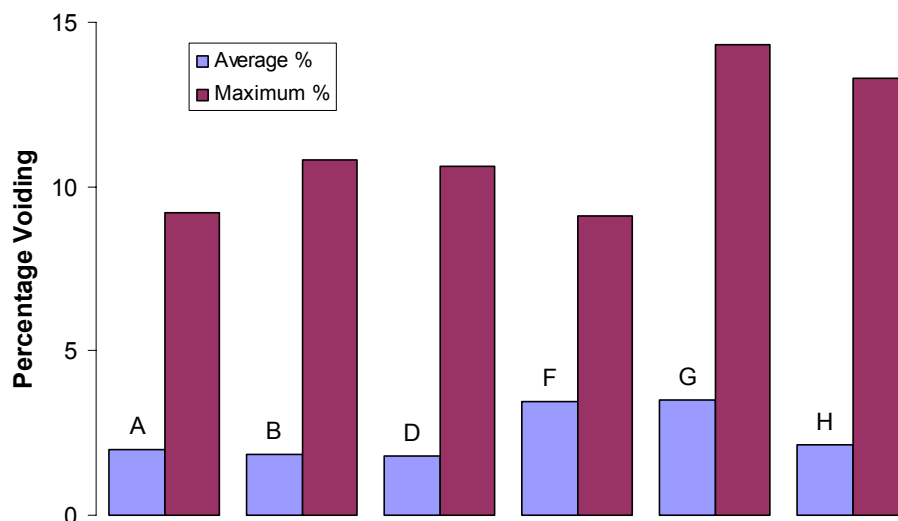


Figure 12: Comparison of average and maximum BGA voiding for six pastes using profile 3

Figure 13 demonstrates the effect of profiling on the voiding levels of three different paste types from a single manufacturer. Profiles 1, 2 and 3 have progressively faster times to peak temperature, the intention being to reduce the amount of pre-heat on the paste and increase the level of volatiles present during reflow. Again there was little difference between the pastes or the profiles with average voiding levels only varying between 1.8 and 3.3%, with the largest voiding in any ball varying between 9 and 13%. Again all of these voiding levels are well below the 25% maximum voiding level specified by IPC (Reference 13).

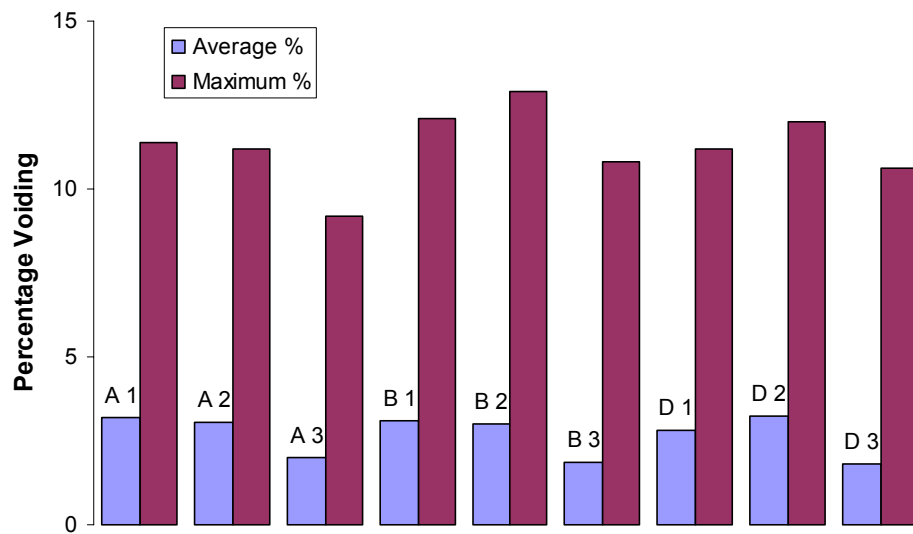


Figure 13: Comparison of average and maximum BGA voiding for three pastes using profiles 1, 2 and 3

The effect of ageing the PCB prior to assembly is presented in **Figure 14**. In this case, PCBs were aged by passing them through a lead-free reflow profile (up to 4 times) prior to solder paste deposition, the intention being to reduce the solderability of the solderable surfaces. This was undertaken for 2 pastes (A & B) and for two profiles (2 and 3). Again, the levels of voiding differed little between the samples. Average voiding varied between 1.8 and 3.5% with the largest voiding in any one ball varying between 9 and 13%. Again all of these voiding levels are below the 25% maximum voiding level specified by IPC (Reference 13).

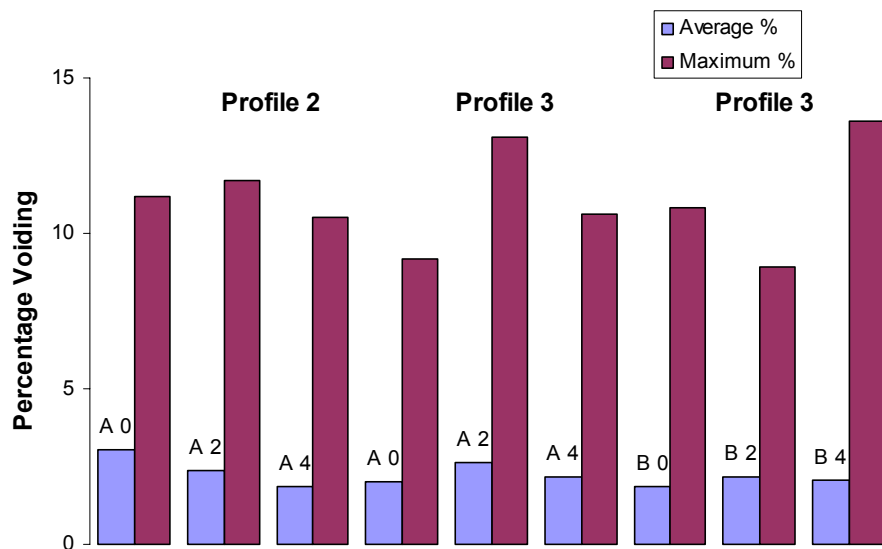


Figure 14: Comparison of average and maximum BGA voiding for two pastes using three levels of pcb preconditioning (0, 2 and 4 bare-board reflow passes)

Figure 15 demonstrates the effect of preconditioning water-soluble solder paste by subjecting the printed paste to an extended period of damp heat (4 hours at 40°C/93%RH). With both profiles, average and maximum voiding did increase with preconditioning but the greatest average voiding level was only 2.8%, with the greatest voiding in any ball still being less than 15%. All of these voiding levels are well below the 25% maximum voiding level specified by IPC (Reference 13).

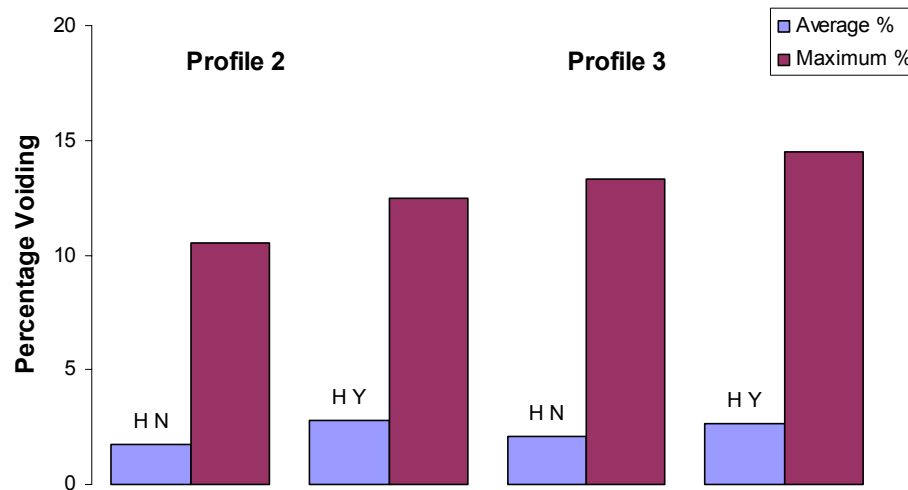


Figure 15: Comparison of average and maximum BGA voiding for water soluble paste without (n) and with (y) damp heat conditioning before reflow

As a result of this work, in which seven different solder pastes have been evaluated with 3 reflow profiles, end-users can have a high degree of confidence that voiding levels in lead-free solder pastes can be kept below the IPC specified maximum of 25% by area.

4.2 PHASE 2 VOIDING LEVELS

From the phase 1 results, three different profiles were chosen to give low, medium and high voiding levels.

4.2.1 R0603 Voiding Levels

Example images for the L, M and H assembly sets are presented in **Figure 16**. Whilst autocalculation of voiding levels of these components was not possible, it is clear that in common the PBGA results, voiding levels in the R0603 components are generally low, with voiding levels increasing from L through M to H levels.

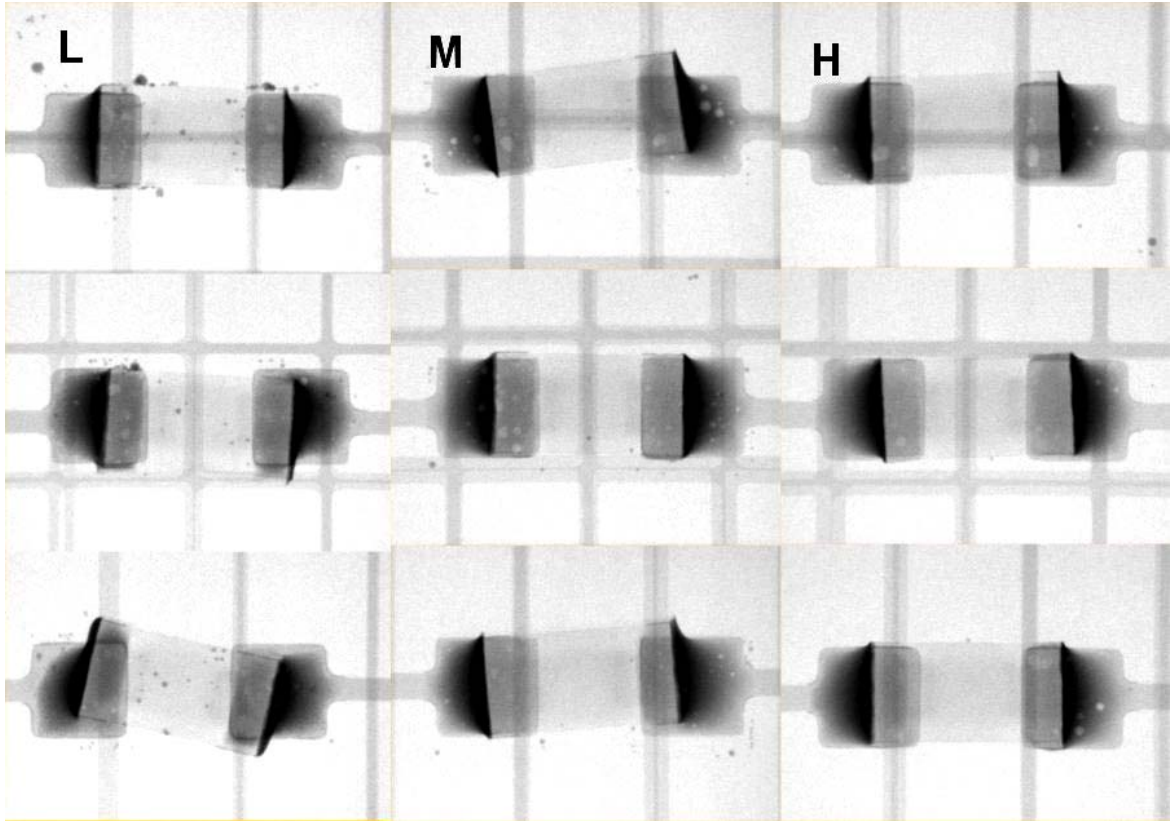


Figure 16: Example images of R0603 for L, M and H voiding levels

4.2.2 R1206 Voiding Levels

Example images for the L, M and H assembly sets are presented in **Figure 17**. As with the R0603 components, autocalculation was not possible, but again it is clear that in common with the R0603 and PBGA results, voiding levels in the R1206 components were generally low, with voiding levels increasing from L through M to H levels.

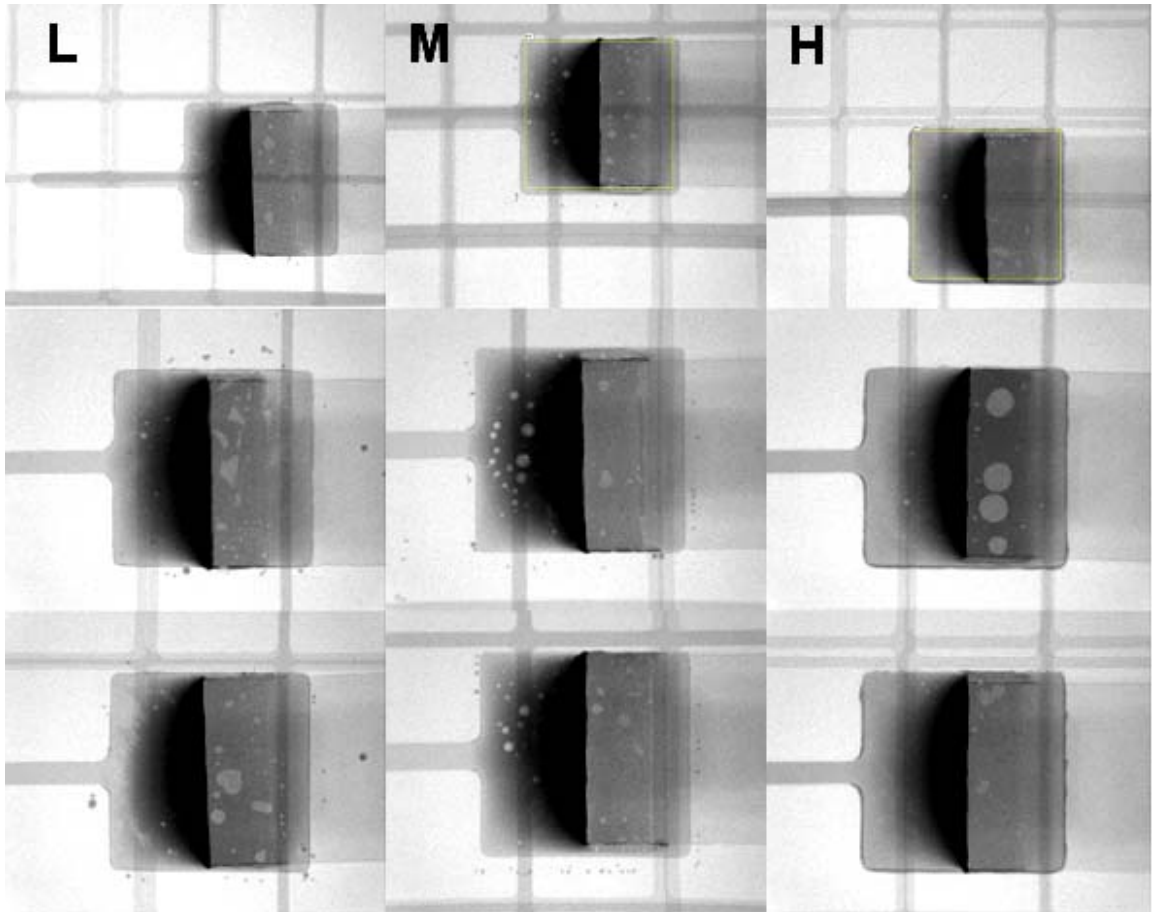


Figure 17: Example images of R1206 for L, M and H voiding levels

4.2.3 SOIC Voiding Levels

Example images for the L, M and H assembly sets are presented in **Figure 18**. As with the resistor components, autocalculation of voiding levels was not possible, but it is clear that voiding levels in the SOIC components were generally low, with little difference between the L, M and H levels.

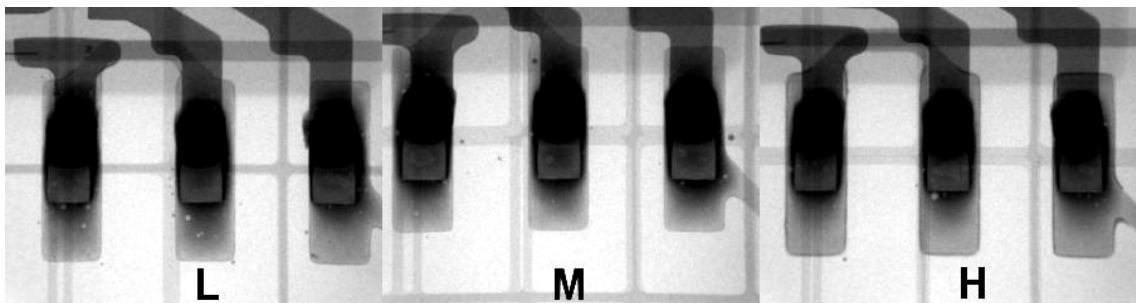


Figure 18: Example images of SOIC for L, M and H voiding levels

4.2.4 PBGA Voiding Levels

The results for the PBGA components from the three profiles in manufacturing ten identical assemblies are shown in **Figure 19**. All these profiles produced voiding levels less than the maximum 25%, permitted by the IPC A610 visual inspection guidelines (Reference 13). IPC 7095 (Reference 5) assembly and inspection guidelines for BGAs, call for a more stringent maximum voiding level than IPC A610. This maximum level is 9% on a sample basis for voids within the joint after reflow. Using angled transmission X-ray inspection, the location of the voids created in these samples was determined to be in the bulk solder of the joints. Thus from **Figure 19**, it can be seen that all three sets of samples contained individual voids greater than 9%, but the occurrence of these is infrequent, and being less than 1% of all voids for each set. Set H has the highest level of voiding over 9% with 0.5% of voids being above this figure. Example images of PBGAs from each voiding level are presented in

Figure 20.

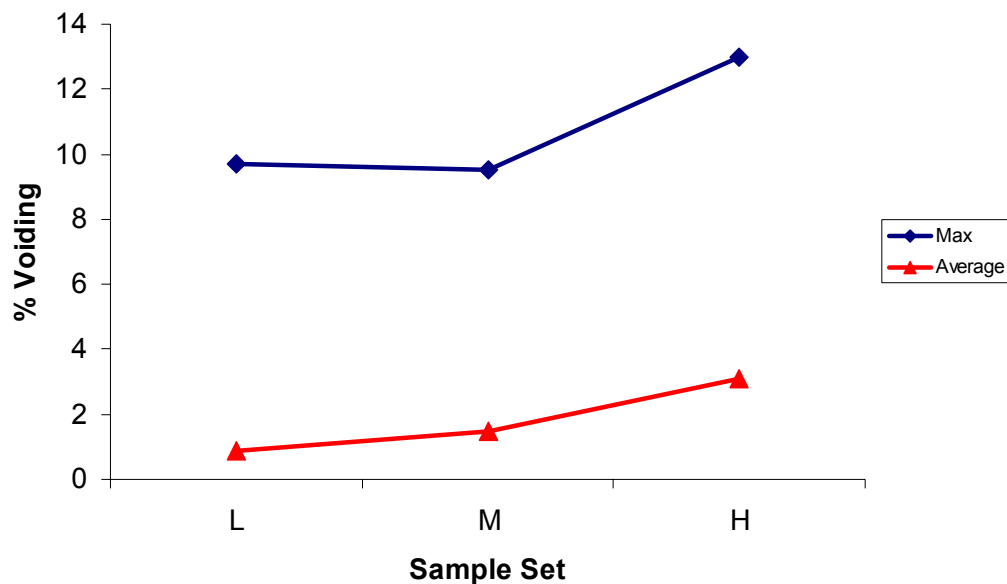


Figure 19: Comparison of average and maximum voiding levels for phase 2 samples

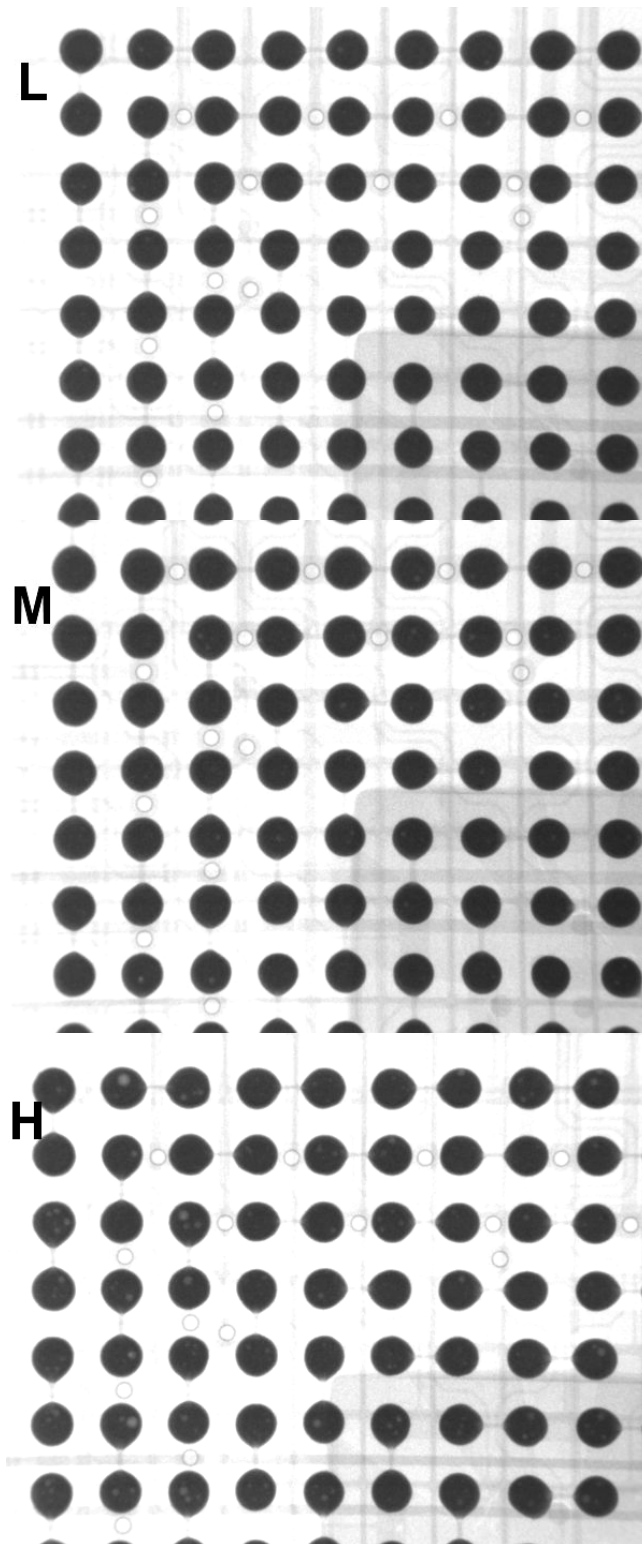


Figure 20: Example images of PBGA for L, M and H voiding levels

Figure 21 provides a typical distribution of void sizes in a PBGA from the H set of samples. Voids greater than 9% are highlighted in red. **Figure 22** shows the position of the component on the test board. High void density in the PBGA is greater towards the

front edge of the PCB (right side of the device), where joints would be expected to reach a higher temperature, and reach that temperature more quickly.

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	Q	R
1	3.3	0.2	2.0	3.9	3.5	2.1	2.5	0.2	1.4	1.1	2.5	4.1	5.2	6.5	4.2	6.1
2	4.4	0.0	3.8	0.0	8.3	2.0	1.1	2.9	5.2	2.1	2.8	1.6	3.2	1.6	4.2	2.6
3	0.0	1.4	2.6	4.2	3.9	4.9	1.3	3.2	3.1	3.3	2.8	3.9	3.7	0.0	7.7	6.8
4	1.8	1.9	7.1	1.4	0.9	1.6	6.0	4.1	2.8	3.5	1.4	4.7	5.7	3.7	2.6	1.5
5	2.3	2.2	2.3	3.2	1.9	1.0	2.7	6.6	4.0	3.3	0.0	1.3	3.3	1.7	6.3	1.8
6	4.5	2.6	0.4	2.1	3.6	0.0	0.9	2.0	5.6	4.2	1.6	2.1	0.4	6.0	0.8	3.2
7	0.6	0.0	2.0	4.0	2.6	0.7	0.7	0.7	1.5	4.0	2.7	2.3	1.4	4.5	2.4	6.2
8	0.0	7.5	2.2	1.0	3.6	6.1	0.6	0.9	6.3	1.0	0.0	4.8	1.1	7.0	0.0	2.6
9	7.9	3.3	2.9	1.8	0.4	0.7	0.2	3.1	0.9	3.6	3.8	3.2	1.0	10.8	1.2	9.0
10	5.9	1.1	0.9	1.5	4.8	3.2	0.0	2.8	5.0	0.0	1.2	2.6	3.0	0.3	4.0	3.3
11	4.0	2.0	1.5	0.0	2.7	5.4	3.1	1.3	0.0	1.3	2.3	0.0	0.0	6.1	0.3	1.7
12	1.2	2.0	2.9	5.8	0.0	0.5	0.0	3.2	3.0	4.0	4.8	0.0	0.3	1.6	0.8	5.2
13	2.2	0.3	0.0	1.4	0.0	3.6	0.6	4.6	1.0	6.9	0.3	1.9	0.3	0.0	6.9	4.4
14	1.6	1.9	1.9	0.8	2.2	2.3	0.0	1.6	1.3	0.2	2.3	0.3	1.5	0.8	2.2	2.1
15	0.3	3.7	0.0	8.0	1.7	0.3	5.5	2.8	0.2	2.7	1.1	2.2	6.0	3.4	1.0	1.7
16	3.0	2.3	1.9	2.9	1.0	2.4	1.1	1.7	3.7	1.9	1.4	2.7	3.9	6.1	0.4	9.6

Figure 21: Distribution of void sizes in PBGA on typical H sample

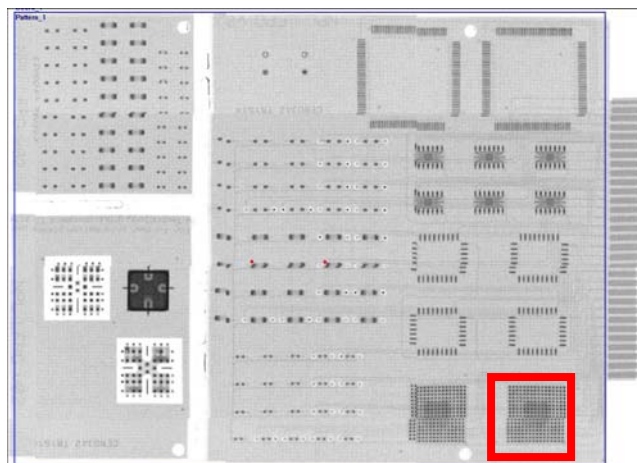


Figure 22: Position on test board of PBGA featured in Figure 21

4.3 ELECTRICAL TEST FAILURES

4.3.1 R1206 Failures

Figure 7 shows the comparison of the electrical failures for R1206 components. These three data sets show very little difference, indicating no apparent change in reliability for the voiding levels generated.

4.3.2 R0603 Failures

These failures are somewhat higher than would normally be expected for this component type after 2000 thermal cycles. This may be due to via failures, which could not be eliminated from the data as the vias within the electrical test circuit were sited close to the component joints and could not be probed reliably without affecting the soldered joints. Figure 6 shows that the failures for the low and medium voiding levels for the R0603 components were significantly greater and initiate earlier than for the high voiding levels. This may be a result of premature via failures, with these two longer profiles causing greater damage to vias. Alternatively, the greater number of voids in the H samples, may be acting as crack arrestors. The inclusion of voids within these joints may increase the height of the solder joints (possibly by as much as 4%). This will reduce the stress on a joint for the same joint strain, compared to shorter joints in the other low data sets. It may simply be that the greater number of the voids, making the structure more flexible, affects the mechanical properties of these joints. The lack of differentiation between the three sets of R1206 components, combined with the similarity in shear strength and shear strength deterioration, indicates via failures are probably the dominating causes for the changes in reliability for these components.

4.3.3 PBGA Failures

All PBGA failures occurred in the C-rings. These are the rings immediately adjacent to edge of the silicon die (represented by the shaded area in **Figure 8**). Here the TCE of the device is constrained by the low TCE of the die, and the difference is at a maximum from the TCE of the substrate. Because of this difference and the distance from the centre of the device, joints in this region are subjected to the most strain, and are therefore likely to be the least reliable. However, after 2000 thermal cycles, there is little difference between the reliability of the PBGA components in the three data sets. An attempt was made to correlate the occurrence of large voids (greater than 10%) with failures in C-rings of the PBGAs. However, joints with large voids occurred in both failed and reliable interconnection rings. Therefore, the position of a joint and its proximity to the edge of the die, have much greater significance than the levels of voiding investigated in this work.

4.4 SHEAR TEST RESULTS

For the shear tests results for both the R1206 and R0603 components as shown in Figures 9 and 10, there were no significant differences between the shear strengths for any of the three voiding levels.

5 SUMMARY

Although there is much information in the literature to suggest a link between voiding, soldering and reliability of the joints assembled using conventional SnPb solders, there is a paucity of data relating to joints assembled using current lead-free solders. In view of the legislation-driven change by the industry to lead-free technologies, the work reported here was undertaken to investigate the possibility of a similar link for joints produced using lead-free technologies.

In Phase 1 of this work, the joints of SM test boards assembled using lead-free solder technologies did not exhibit the high levels of voiding that had been previously associated with conventional SnPb soldering. These low voiding levels were consistently encountered across a wide range of applied lead-free solder technologies, but all the voiding levels recorded were well below the permitted levels (25% by area) in IPC A610 revision D. Average values were in the range 2-4%, although individual values reached 13%. No paste exhibited voiding in any PBGA joint >15% by area despite attempts deliberately to induce higher voiding levels. This robustness of the lead-free technologies will be welcomed by industry and ease its current worry that lead-free solder pastes might be prone to high voiding levels.

The three levels of voiding available for Phase 2 were in the range up to 13% by area, and test boards were subjected to extensive thermal cycling (2000 cycles from -55 to +125°C). However, there were no discernable differences in the reliability of the joints as monitored using (a) electrical resistance, (b) shear strength, or (c) shear strength deterioration during thermal cycling. Since the IPC 7095 guidelines for class 3 BGAs call for a maximum voiding level of only 9%, the results clearly suggest that if the IPC maximum voiding levels are adhered to, there will be no adverse effect from voiding on the reliability of lead-free solder joints.

6 CONCLUSIONS

- *SM assembly using lead-free solder technologies processed under a wide range of conditions has not produced high levels of voiding.* This robustness of the lead-free technologies will be welcomed by industry and ease its current worry that lead-free solder joints might be prone to high voiding levels.
- Earlier work (Reference 14) had demonstrated that with solder joints assembled using conventional SnPb alloys, it was possible to incur high levels of voiding (<20% by area). However, in the present work it has not been possible to produce such high levels of voiding. *All the voiding levels recorded were well below the permitted levels (25% by area) in IPC A610 revision D.* Average values were in the range 2-4%, although individual values reached 13%.
- These low voiding levels were consistently encountered across a wide range of lead-free solder technologies. The evaluation involved seven solder pastes (six no-clean; one water-soluble) from three suppliers processed through a range of reflow profiles. In addition, some of the PCB test boards had been subjected to

artificial ageing, and the water-soluble paste had been subjected to damp-heat ageing, in an attempt to produce “worst case” conditions.

- The three levels of voiding available for Phase 2 were in the range up to 13% by area, and test boards were subjected to extensive thermal cycling (2000 cycles from -55 to +125°C). However, there were no discernable differences in the reliability of the joints as monitored using (a) electrical resistance, (b) shear strength, or (c) shear strength deterioration during thermal cycling. Since the IPC 7095 guidelines for class 3 BGAs call for a maximum voiding level of only 9% (cf 25% for IPC A610) the results clearly suggest that if the IPC maximum voiding levels are adhered to, there will be no adverse effect from voiding on the reliability of lead-free solder joints – a conclusion that will be welcomed by manufacturers and end users of lead-free assemblies.

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