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Crack Detection Methods For Lead-free Solder Joints

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ABSTRACT

This report describes an investigation into the suitability of a number of techniques used to study cracking in lead-free solder joints, and hence their use in assessing joint lifetimes. Cracks were induced into the solder joints of chip resistors on FR4 substrates, and studied using metallographic micro-sectioning, dye penetration, mechanical test and thermal conductivity techniques. The work has shown that those techniques traditionally used to study lead-based solder joints can readily be used for assessing lead-free solder joints The traditional micro-sectioning method is suitable for locating and imaging the solder joint crack, especially when the section is examined in a SEM. However, it is not very suitable for quantitative analysis of cracks or their detection in small surface mount resistors. Dye penetration techniques allow a better characterisation of cracks in the horizontal plane and can provide a quantitative measure of the cracked surface area. Shear testing is a proven destructive method for evaluating not only the degree of crack propagation and damage to the solder joint, but also the general strength of the joint. The other methods studied (3 and 4-point bend tests, pull test and heat transfer) have severe limitations and are currently unsuitable for studying cracks in the solder joints of electronic assemblies, requiring further development.

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Approved on behalf of Managing Director, NPL, by Dr C Lea,
Head, Materials Centre

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1. Introduction

In electronics assemblies components and substrates are mechanically and electrically interconnected via soldering processes, and since the solder joint is the weakest point in the assembly, it usually determines the lifetime of the assembly. Hence estimates of the lifetime of electronics assemblies are often made by monitoring the degradation (and eventual failure) of solder joints under severe service or accelerated conditions. Such estimations of the joint lifetimes are also desirable, if not necessary, for feedback to achieve and maintain good process control, especially for high reliability applications. There are several investigatory techniques which are used to study conventional SnPb solder joints, and which are therefore potentially suitable for providing data on the lifetime of lead-free solder joints. Previous work [1] on mechanical studies of solder joints has demonstrated that mechanical failure of the joint does not happen in a sudden, catastrophic manner, but occurs as a gradual change, usually in the form of cracking. Typical cracking of a solder joint of a 2512-type chip resistor is illustrated in Figure 1.

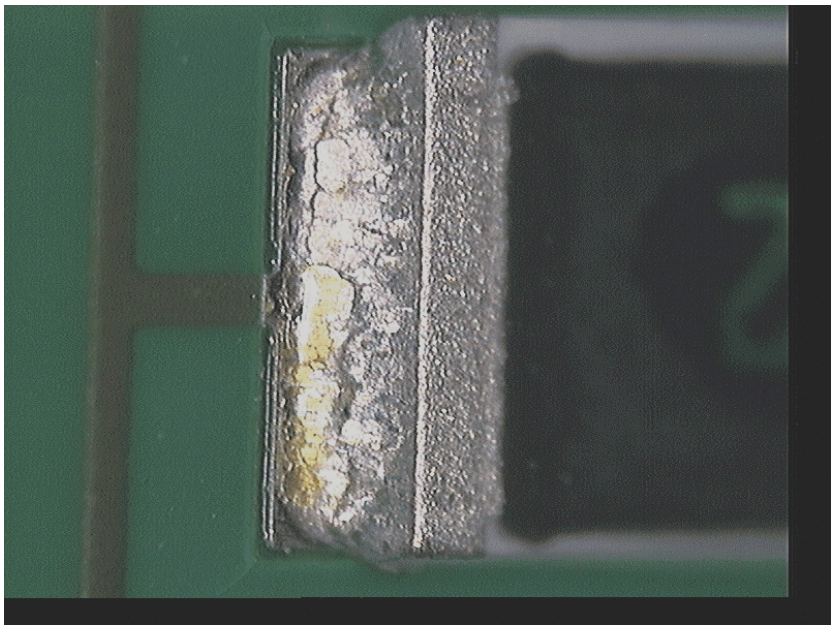

Figure 1. A 2512-type chip resistor showing cracking in the solder joint.

The work reported here has investigated the suitability of a number of these techniques to study cracking in lead-free solder joints, and hence their used in assessing joint lifetime. The techniques studied included micro-sectioning, dye penetration, mechanical tests, and thermal conductivity. Where appropriate FEA analyses have been undertaken to aid in assessing the various tests.

2. Test Specimens

The strength of the solder joints is particularly affected when the assembly contains large components with rigid ceramic bodies soldered to FR4 laminates. In consequence, in order to

simulate this "worst case" scenario, 2512-type chip resistors and FR4 substrates with the ENIG (immersion gold over electroless nickel) finish were used in this study. They are lead-free, in common usage, and widely available. The PCB assemblies used, illustrated in Figure 2, were fabricated from single-sided FR4 boards (thickness 1.6 mm) with a copper thickness of 35 µm (copper plating 1 oz/sq.ft) and an ENIG board finish.

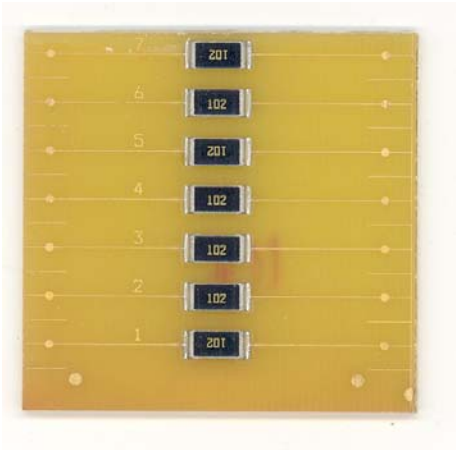

Figure 2. FR4 laminate with 2512-type resistors used in the crack assessment study.

The substrates were stencil printed with solder paste using a stainless steel stencil with a thickness of 150 µm (0.006"). The components were placed onto the substrates using an automatic placement system, and the lead-free solder alloys used were 95.5Sn3.8Ag0.7Cu and 96.5Sn3.5Ag in no-clean solder paste compositions. These processes ensured a consistent solder joint volume. Reflow of the solder paste was achieved in a convection reflow oven - the reflow temperature profiles are described in detail elsewhere [2].

3. Thermal Cycling

The traditional acceleration method of generating cracks in solder joints is to subject the assemblies [3] to thermal cycling regimes, during which the cracks are caused by stresses exceeding the ultimate shear stress of the particular solder alloy. The localised stresses can be caused mechanically, by material displacement, or by mismatch of the coefficients of thermal expansion (CTE) of the two joined materials exposed to temperature changes. In the electronic assemblies used here there were mismatches in CTE between the component body (alumina 6.5ppm/°C), the solder (21-25ppm/°C), the copper termination pad (17.6ppm/°C) and the FR4 laminate (CTE_{xy} = 12-18ppm/°C, CTE_z = 50ppm/°C). In addition, all these coefficients vary with temperature. The largest mismatch over the longest absolute dimension is between the component body and the FR4 substrate [4]. The parameters of the thermal cycling regime used in this evaluation study are listed in Table 1, and Figure 3 shows a graphical representation of a thermal cycle.

Table 1: Tested temperature cycling regimes within ± 4°C of the set value

Cycle	Low temp	High temp	Ramp	Dwell	Period
	[°C]	[°C]	[°C/min]	min	min
A	-55	125	10	5	45

This thermal cycling test regime is that widely used in military applications testing, which accounts for the wide temperature range of the cycle. The ramp rate of 10°C/min is a moderate ramp rate, slower than a thermal shock regime, which is typically above 30°C/min [3]. The relatively short dwell time of 5 minutes is to minimize the cycle period and shorten the test period.

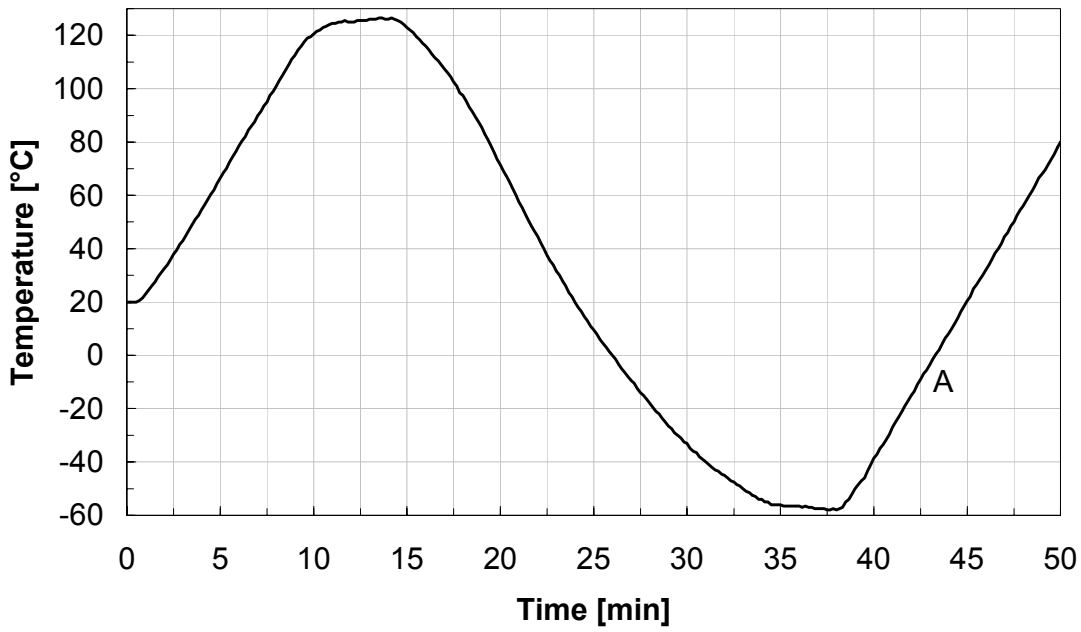

Figure 3. The thermal cycle used in this work.

4. Micro-sectioning

In order to study both the joint microstructure and any cracking that occurs, it is essential to examine carefully prepared microsections of suitable joints.

In consequence, assemblies of component and substrates were pre-cut using a low speed saw to avoid causing any additional stressing, and these pre-cut specimens were mounted in cold curing epoxy resin moulds to protect and encapsulate the solder joints. The specimens were ground using successive grades of silicon carbide papers (120 to 4000 grit), followed by polishing using diamond pastes/sprays with successive particle sizes from 15 to 0.25 µm in diameter. Due to the differences in hardness of the solder, the copper pad, any interlayer present, and the component edge, care was exercised to ensure that only a light pressure was used during polishing. Diamond impregnation of the polishing cloth was kept to a maximum to ensure an optimum cutting rate.

Final polishing of the samples was carried out by hand using a gamma aluminide powder suspended in lapping fluid (OP-S).

When etching of the samples was required, for example to highlight microstructure, the following procedures were used:

Lead based solders: a solution containing 2 ml hydrochloric acid and 98 ml industrial methylated spirits in a polish-etch technique, employing 0.25µm diamond paste as the polishing medium.

Lead-free solders: 2 ml nitric acid, 2 ml hydrochloric acid and 96 ml distilled water in a polish-etch technique, with 0.25µm diamond paste as the polishing medium. For satisfactory results a very short polish cycle (2 sec) was applied followed by immediate specimen wash in distilled water.

Acceptable images highlighting *joint microstructure* were obtained using an optical microscope, whereas *cracks* in the solder joints were usually better located using an SEM in the secondary electron mode. However, the SEM technique does require a conductive coating (e.g. AuPd, Au or carbon) over the specimen. The level of polishing was minimised by examining the specimens in the SEM back scattered electron mode, which is well suited for qualitative and/or quantitative analyses. A technique called "digimap" (i.e. mapping selected elements in distinguishable colours) also proved to be helpful when used in applications with coatings and laminate.

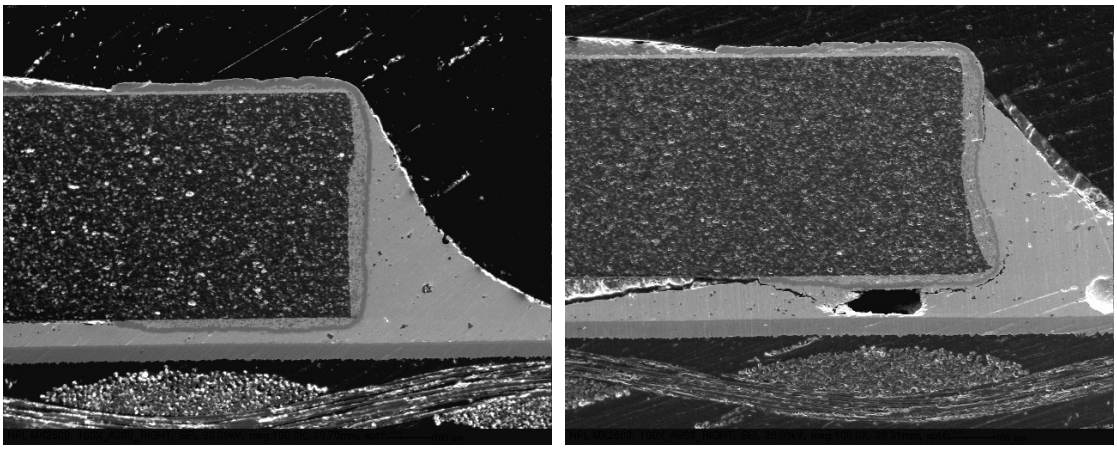

Figure 4. Microsections of 2512-type resistor solder joints without a crack (300 cycles - left) and cracked (900 cycles - right). The images were taken in the SEM secondary electron mode

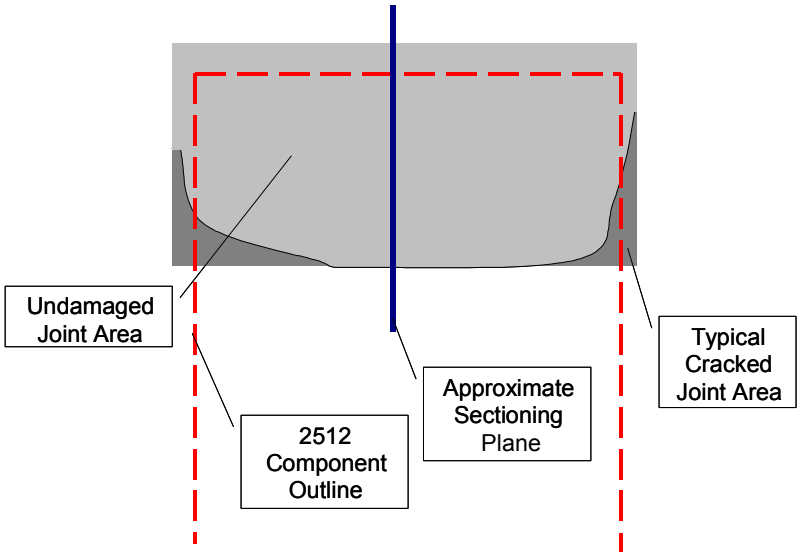

Figure 5. Central sectioning point shows the microstructure, but not developing corner cracks.

It should be noted that whilst the micro-sectioning technique is suitable for the assessment of the failure mode, it can be misleading for quantitative evaluation of crack growth in the solder joints. This is illustrated in Figure 5, which shows the location of cracked joint areas with reference to a mid plane between the ends of the component. If the latter happens to be the cross-sectional plane none of the cracked area would be visible in the microsection. Hence to ensure crack detection the cross-sectional plane should be close to the component outline. Unfortunately with small component sizes, such as 0805-type resistors, this may be difficult to achieve.

5. Dye Penetration

Dye penetration is another destructive technique used for studying the location and extent of cracking. In this study the dye penetration test was performed on the 2512-type resistor joints after thermal cycling. The assemblies were cleaned in an ultrasonic bath in a solution of 50% water, 50% iso-propyl alcohol. After drying the assemblies using compressed air, they were inserted into a vacuum bell and immersed in Rocol Layout Ink Fluid (red or blue) dye. A partial vacuum was applied for 15 min. The dye was cured on the assemblies by baking in a convection oven at 50°C for 10 minutes. The components were then removed by twisting with pliers, and the joints inspected for dye penetration using an optical microscope. A typical image is presented in Figure 6, in which the white line highlights the cracked area.

Figure 6. Crack in a SnAgCu solder joint after thermal cycling.

The crack area growth in terms of the number of cycles was evaluated by measuring the number of pixels in the appropriate part of the image, and the results are presented in Figure 7. Since this method gives more quantitative results than does micro-sectioning, it can be used for assessment of non-cracked area i.e. to study the stress acting on a solder joint, and to analyze the whole area of a crack. It is not dependent on the positioning of the cross-sectional plane, as is the case with micro-sectioning.

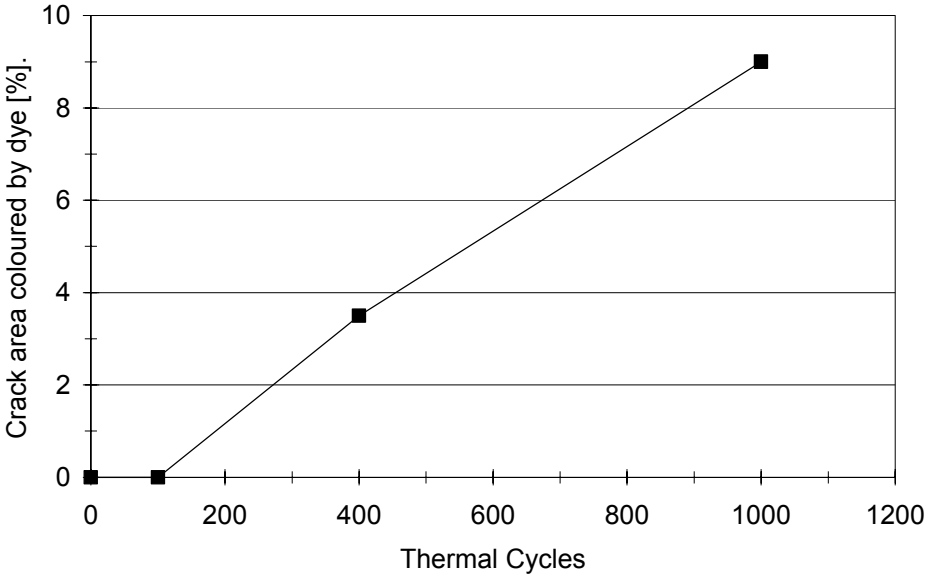

Figure 7. Percentage of cracked area under 2512-type resistors as a function of the number of thermal cycles, for SnAgCu solder

6. Mechanical Tests

Mechanical tests were used to investigate the time-dependent deformation (displacement) of the solder when exposed to an external load. The tests were carried out on surface mount resistors soldered to a FR4 laminate, and measurements were made after 0, 300, 600, 900 and 1200 cycles. The configuration of the test specimen and the materials used are shown schematically in Figure 8.

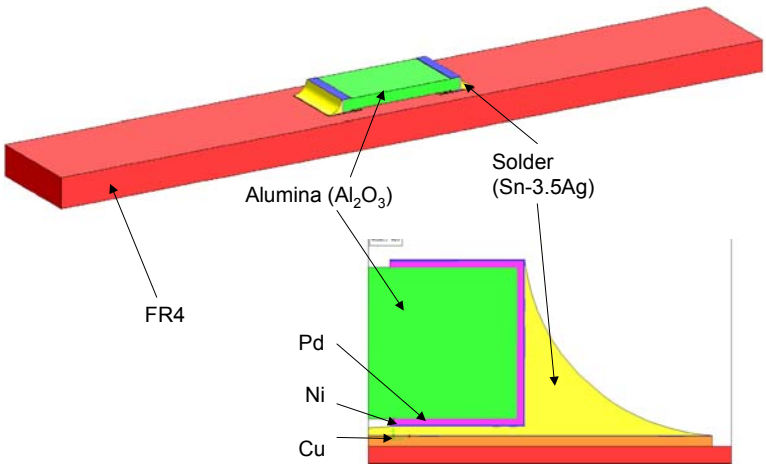

Figure 8. Schematic of test specimen.

6.1. Shear Test

Shear testing is an established destructive method for evaluating not only the degree of crack propagation and damage to the solder joint, but also the general strength of the joint. The method is based on the assumption that the presence of a crack in the solder joint, its size and the extent of its propagation, will influence the strength of the joint. Hence a correlation can be established between the strength of the solder joint and joint failures. A typical shear test set up is presented in Figure 9. The tests in this study were undertaken on a Dage Series-4000 modular multi-function bond-tester.

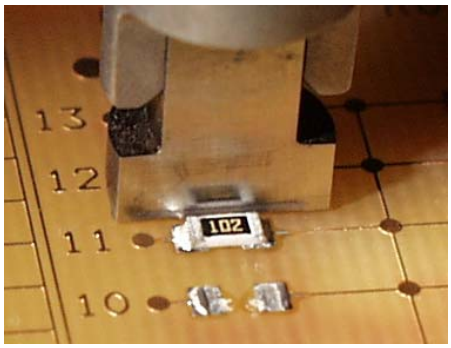

Figure 9. Shear test jig and push-off tool before a shear test

The following steps were carried out:

- The substrate was cut into sections suitable for the shear tester holding jig, using a water-cooled, low speed diamond saw, which produces a clean edge with minimum stress to the board.
- The sections were cleaned (e.g. with iso-propyl alcohol) to remove any contaminant residues from the cutting stage, and dried using compressed air.
- The stand-off height was set at h/2 (typically 80 µm) between the bottom of the shear tool and board surface (h is the stand-off height between the component and the board surface). This is the most important test condition.
- During each test, the shear tool was moved forward at a defined speed (200 µm/s) against the test component, and the applied force increased until the attachment was broken.

The data obtained in the test were analysed in terms of the ultimate shear force required to rupture the solder joint, and then plotted as a function of the number of thermal cycles to which the assembly had been subjected. An average value was calculated from the 26 individual measurements and plotted together with the first and third quartile of a box-whisker diagram shown in Figures 10.

The box-whisker diagrams reveal the distributions of ultimate shear forces measured after reaching a certain number of cycles. Although the testing was performed after a defined number of cycles, the locations of boxes plotted in the diagram have been moved sideways around the nominal number of cycles to avoid overlaying of data. The top and bottom sides of the boxes indicate first and third quartile (Q1, Q3) values of the population sample. The line drawn across a box is an indication of the median (quartile Q2). The vertical lines (whiskers) from these boxes extend to the last data point within the range of the limits. The upper and lower limits are calculated according to the relationships:

Lower Limit: $Q1 - 1.5\,(Q3 - Q1)$, Upper Limit: $Q3 + 1.5\,(Q3 - Q1)$

The circle represents the population mean, and the asterisks (*) are outliers (data points above the fourth quartile or below the first quartile).

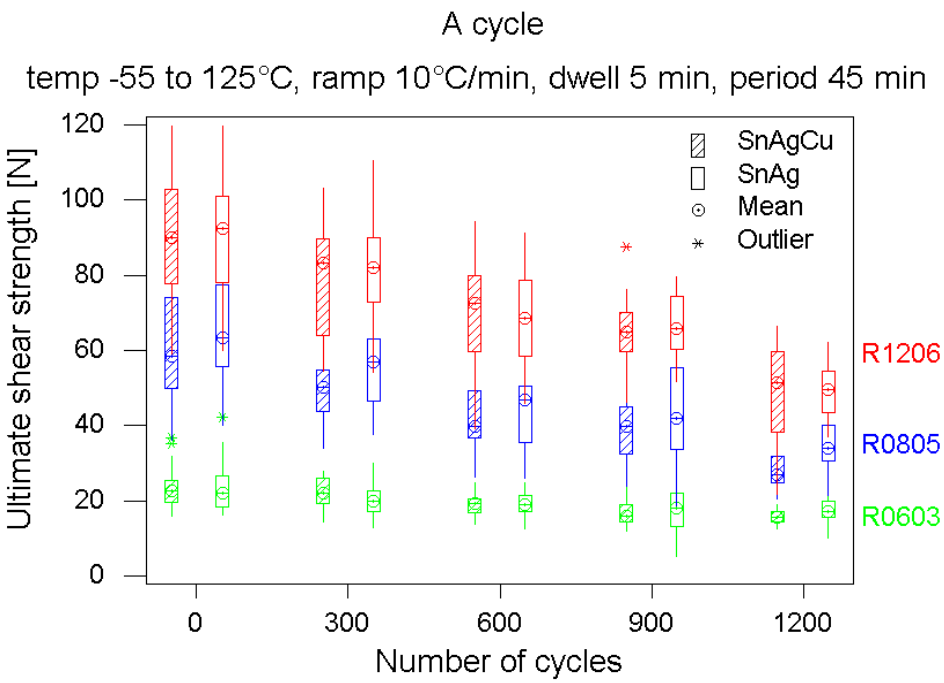

Figure 10. Shear testing results for 3 sizes of chip resistor.

6.2. Pull Test

In the pull test (see Figures 11-13) a constant force of 100N was applied over 20 sec at a rate of 3.3 N/sec and held for 60 sec (Figure 14). The deformation was measured using a strain gauge (Figure 12) mounted on the top of a resistor. Figure 13 illustrates the primary deformation mode of the resistor-substrate system, as calculated using the FEA software tool PHYSICA [5].

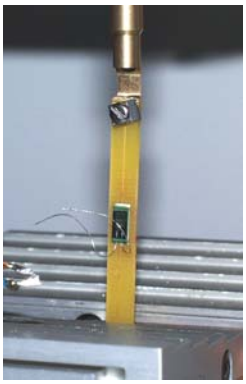

Figure 11. Specimen for pull testing.

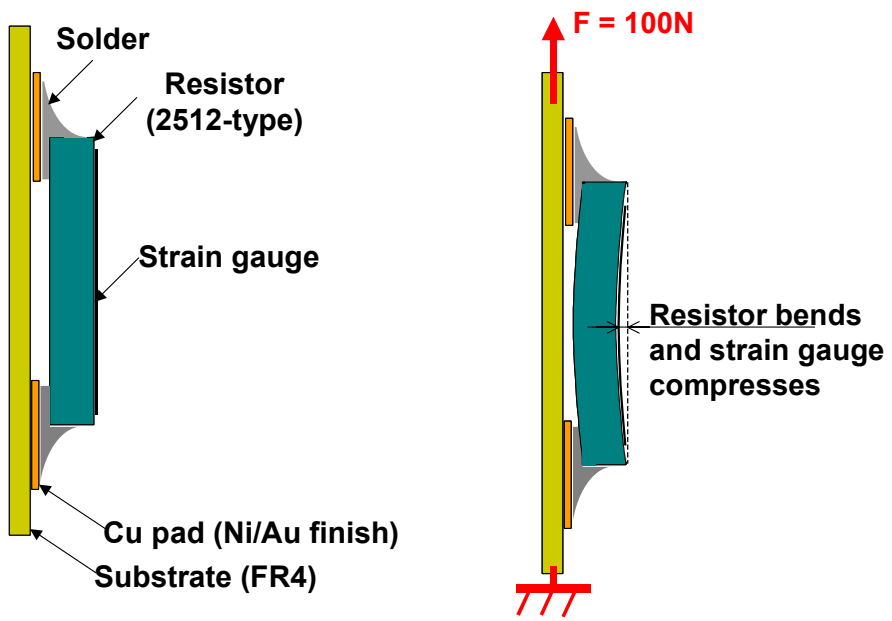

Figure 12. Test arrangements of resistor specimen.

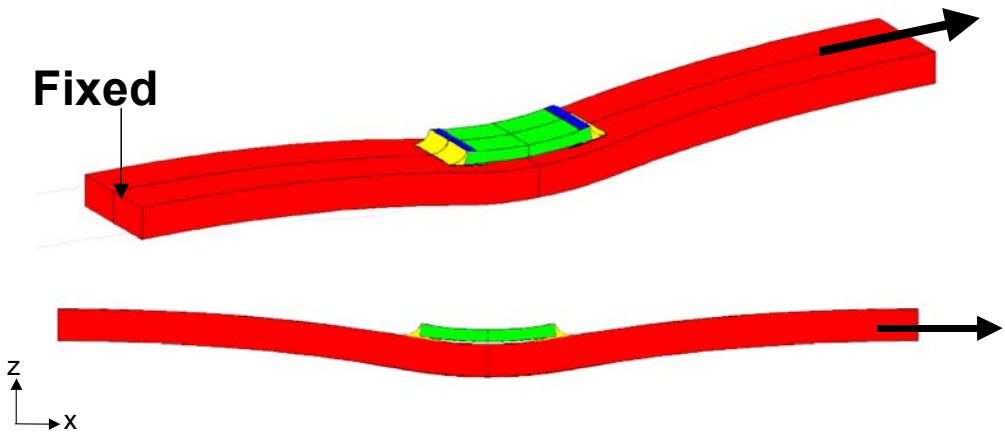

Figure 13. Predicted major bend mode.

The measurements indicate that the solder joint integrity goes through a deterioration phase, and that the top of the resistor is subjected to smaller compression stresses after a high number of cycles.

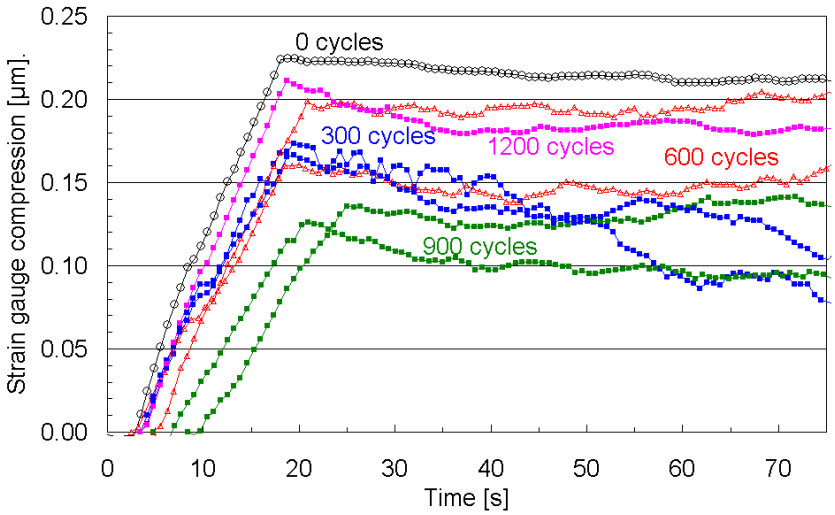

Figure 14. Variation of compression with time.

As shown in Figure 14 the dependence of compression with time does not show the expected steady progression from unloaded (0 cycles) to fully loaded (1200 cycles). This is confirmed in Figure 15 with the non-linearity of the compression as a function of the number of cycles i.e. the compression increases after 1000 cycles for both SbAgCu and SnAg soldered joints. This effect may be associated with the alignment of the specimen, the bonding of the strain gauge, and/or the small resistor joint area. Importantly, however, this method cannot currently be recommended for the assessment of solder joint integrity because of the complications associated with the strain gauge attachment. Better results might be achieved [6] using a field strain monitoring using moiré technique.

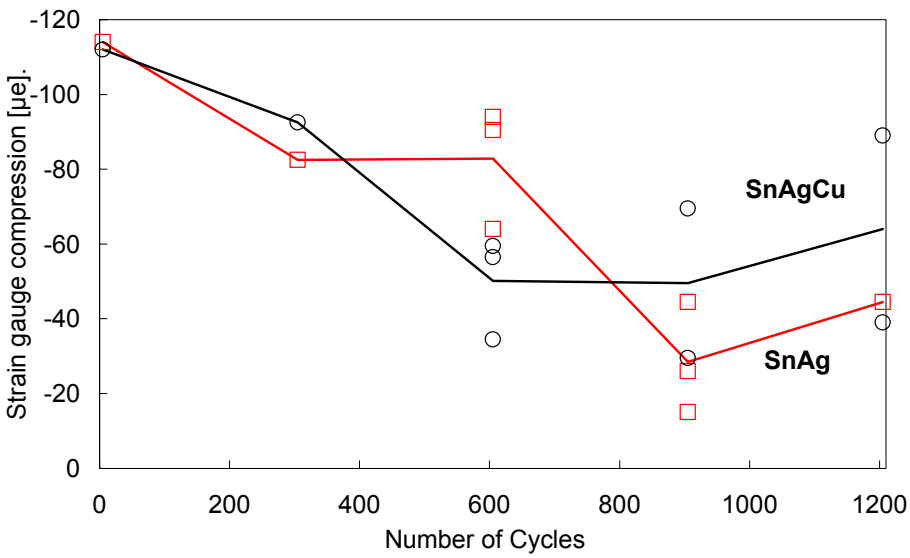

Figure 15. Maximum compression on the 2512-type resistor surface as a function of the number of thermal cycles.

6.3. 3-Point Bend Test

In the 3-point bend test the force was applied to the substrate on the side opposite to that of the resistor (see Figures 16 and 17), and the substrate deformation was monitored and measured at the top of the resistor body. The extent of the deformation depends on the force exerted on the resistor through the solder joint.

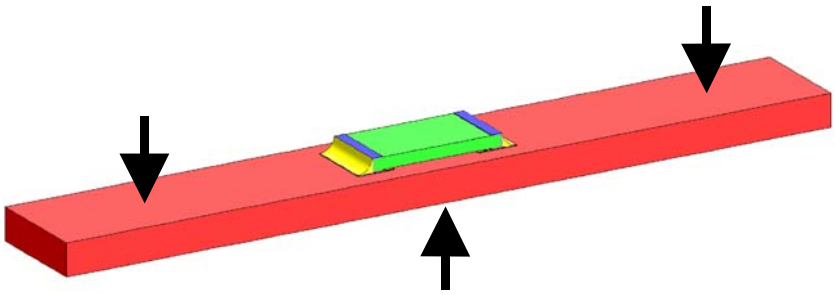

Figure 16. Schematic of the 3-point bend test.

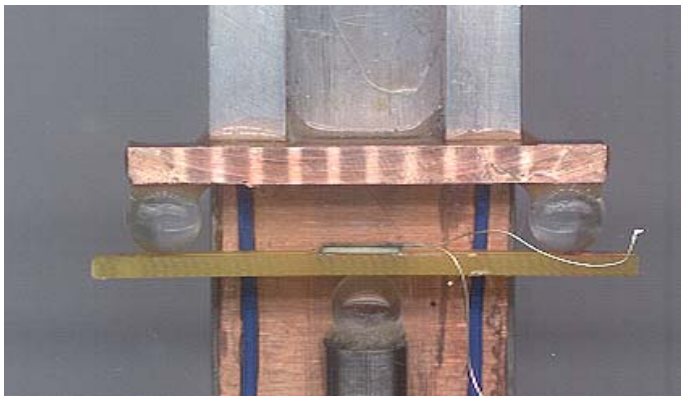

Figure 17. The 3-point bend testing jig.

In Figure 18 the strain gauge measurements of deformation are plotted as a function of the assembly displacement at the mid point between the resistor's soldered joints. The test specimens had been soldered using SnAgCu alloy and had not been subjected to any thermal cycling. This exercise was carried out to investigate the variation of deformation with time after 20 µm displacement steps, each with a dwell time of 10 seconds. The individual displacements are shown along the horizontal axis, whilst the vertical steps represent the amounts of time-dependent deformation after each displacement step. It is clear that after a displacement of only 60 µm the curve takes a step-like shape, indicating a drift in deformation i.e. a time-dependent (creep) behaviour during the 10 seconds dwell period. It follows that irrespective of the thermal cycling

regime used, the solder becomes accommodating and. irreversible plastic deformation (creep) occurs in the joints during the dwell periods of the test. In consequence, the curvature of the bending board becomes such that the gap between the unbending

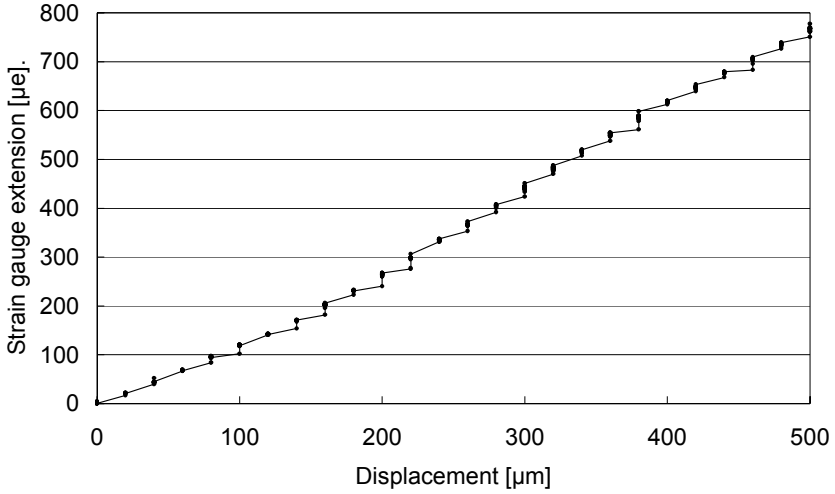

Figure 18. Deformation as a function of incremental mid point displacement of test specimens (SnAgCu, 0 cycles).

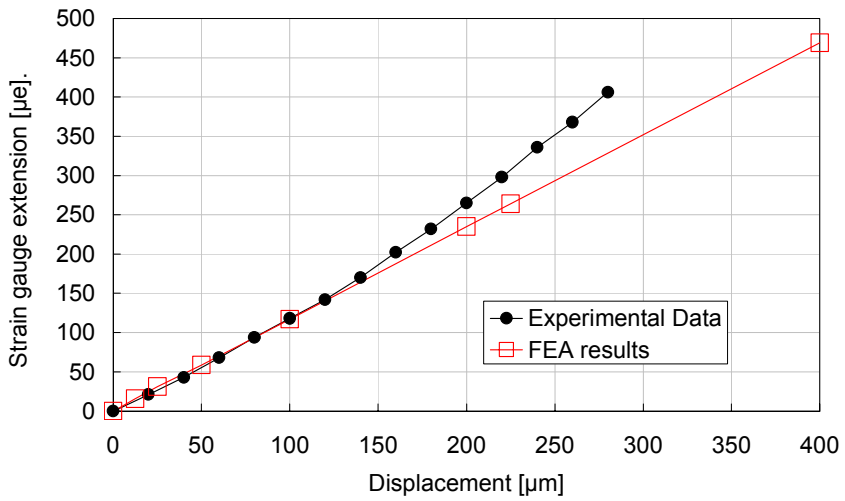

Figure 19. Comparison of experiment data and modelling results for displacement - strain characteristic.

lower face of the resistor and the board itself is closed ands contact may occur. This issue, together with those associated with strain gauge attachment, means this test approach cannot be recommended for assessing cracking or solder joint lifetimes until further development has been undertaken.

Figure 19 shows a comparison between the strain gauge measurement of deformation and a surface strain calculated using an FEA model based purely on elastic deformation. The two

curves coincide for displacements less than ~125 µm. For higher levels of displacement the two curves diverge, and this is attributed to the simplicity of the model. Similar comparisons were made following other tests on specimens subjected to a range of thermal cycles, with similar results.

6.4. 4-Point Bent Test

The 4-point bend test is an alternative to the 3-point bend test, with the solder joints stressed in the opposite direction to that used in the 3-point test. Figure 20 illustrates the layout and the direction of the forces on the assembly. The FEA model calculations were promising (see Figure 21), with a clear relationship showing the influence on the crack length of a theoretical compressive strain on the top-side of the resistor. However, this testing method was rejected as the simulation also highlighted that the practical test would cause further propagation of the cracks and a consequential peeling of the remaining solder joint, as illustrated schematically in Figure 22.

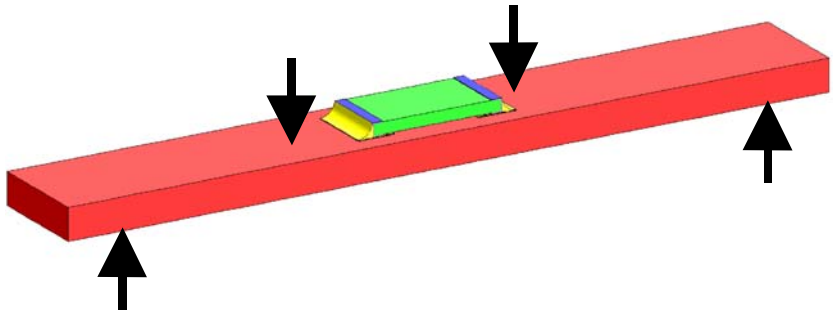

Figure 20. Test specimen with forces (arrows) acting in 4-point bend test.

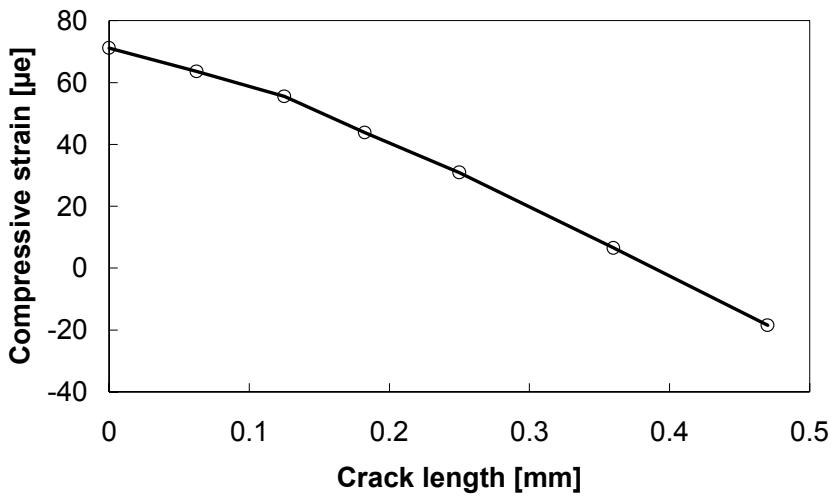

Figure 21. Model calculations of the impact of compressive strain on crack length.

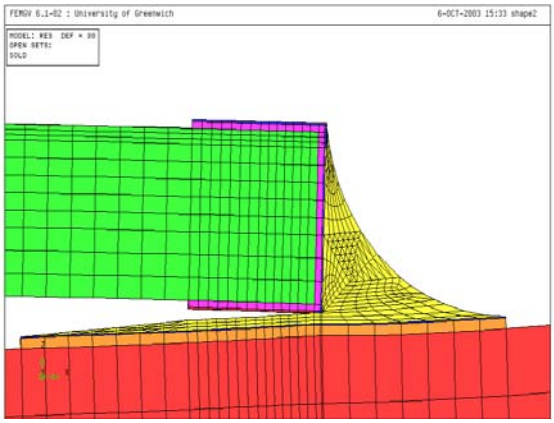

Figure 22. FEA model showing how applied deformation opens a solder joint crack under the resistor termination.

7. Thermal conductivity

It has been suggested that cracks inside the solder joint might affect its thermal conductivity (dynamic temperature change), because as the crack increases the direct conductive path in the material becomes less, resulting in a decrease in the rate of heat transfer. In order to test this suggestion chip resistor assemblies (with thermocouples attached - see Figure 23) having been subjected to various thermal cycling regimes (and hence having various degrees of cracking) were placed on a heated plate, and temperature-time data accumulated.

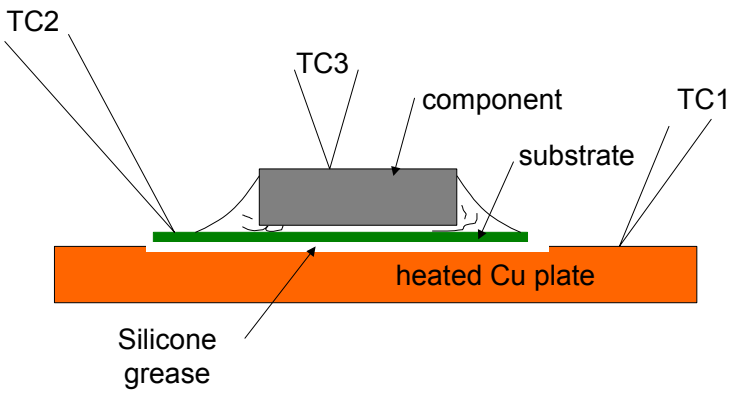

Figure 23. Schematic of specimen arrangement for heat transfer monitoring.

The copper plate was heated to 130°C, and the assemblies (each comprising a PCB substrate with a single resistor chip) were placed onto the plate greased with silicone grease to improve thermal contact. Thermocouple TC1 was used to monitor the temperature of the plate, TC2 that of the substrate, and TC3 that of the top of the soldered resistor. The variations with time of temperatures TC2 and TC3 are shown in Figure 24; they clearly highlight that the resistor temperature (TC3) follows the substrate temperature (TC2) with a short time delay. However, there was no significant difference (see Figure 25) in the time delay for specimens having various

degrees of cracking i.e. those subjected to thermal cycling regimes of 300 or 1200 cycles.

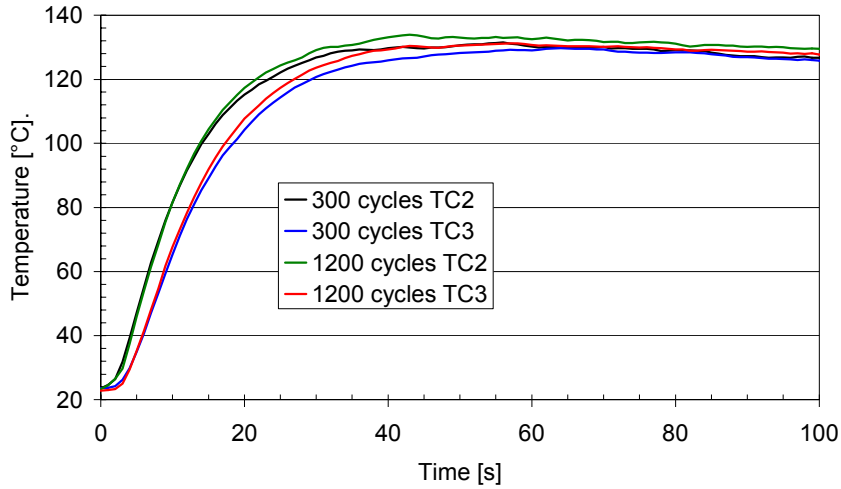

Figure 24. Substrate and resistor temperatures during thermal conductivity tests for specimens subjected to 300 and 1200 cycles.

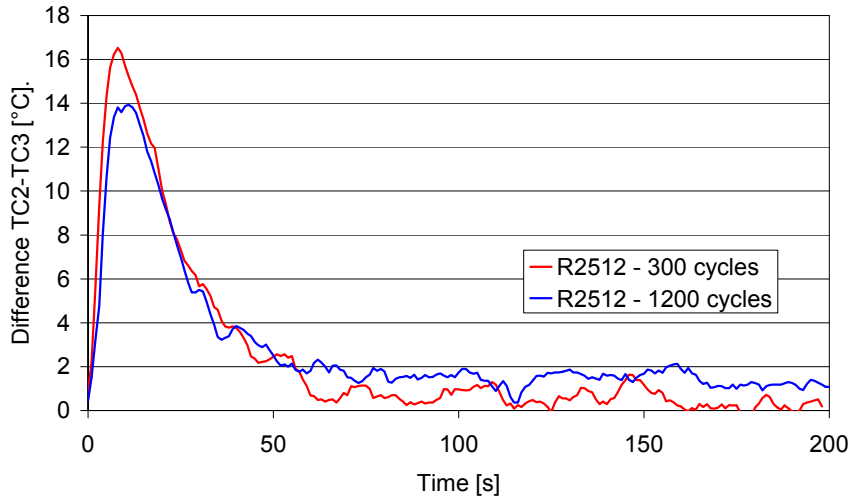

Figure 25. Temperature differences between substrate and resistor.

The experiment was modelled using an FEA approach (see Figure 26). For this the assembly was "exposed" to a heat source (fixed temperature of 100°C) and the temperature on top of the resistor recorded with time.

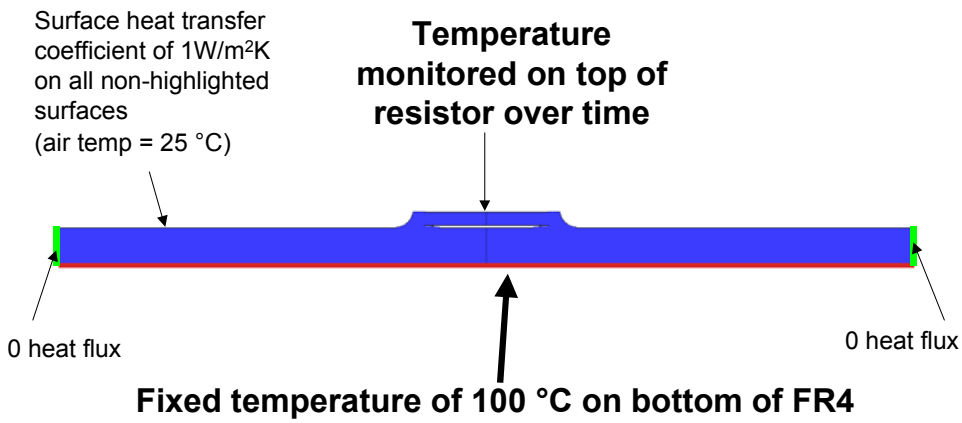

Figure 26. Computer model of heat transfer.

Results from the FEA analysis are presented in Figures 27 A-E, which show solder joints with a range of cracks following heat exposure. The length of each crack is indicated in percentage terms; the 0% crack represents the uncycled, uncracked state, whilst the 100% crack is equal to the length of the resistor termination. Temperatures are indicated by the colours, and the simulations (A-E) were stopped after 12 seconds of heat exposure. It is clear from simulations A to C that there is no significant difference in temperature distributions over the heating up period and hence it is concluded that the size of the crack does not affect the thermal conductivity of the solder joint.

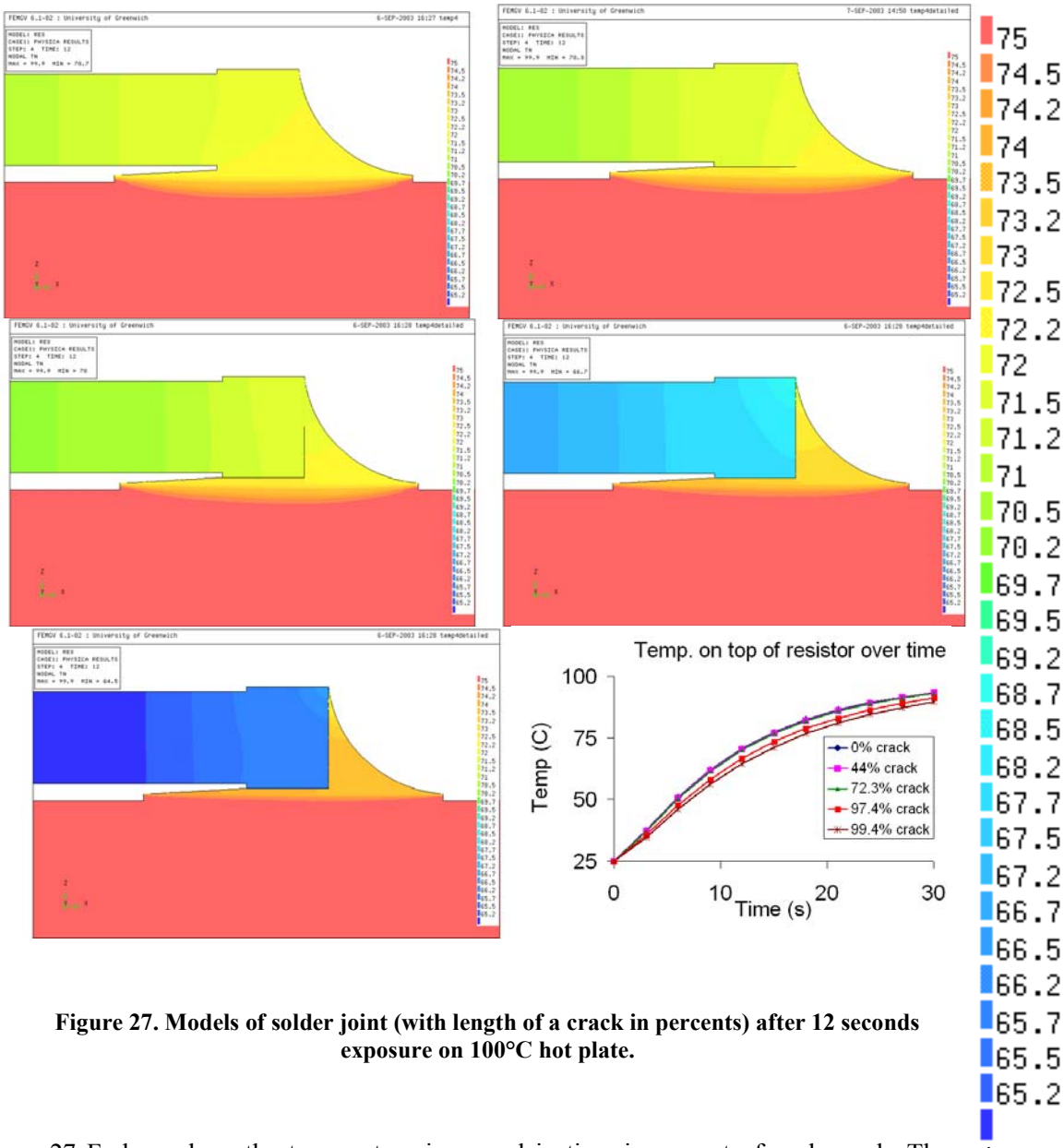

Figure 27. Models of solder joint (with length of a crack in percents) after 12 seconds exposure on 100°C hot plate.

Figure 27 F shows how the temperature increased in time in respect of each crack. The only significant changes in the dynamics of heat transfer occur when the length of the crack is between 72 and 97% of the termination length. However, it is expected that solder joints with cracks of this scale will already be failing mechanically. These results confirm the unsuitability of this testing method in crack assessment.

8. Discussion

A number of investigatory techniques have been assessed for their suitability for study cracking

in lead-free solder joints. The techniques were selected as those in common use (or being assessed) by industry when examining traditional SnPb soldered joints. The work has demonstrated that those techniques suitable for examining SnPb soldered joints are also suitable for examining joints made using the new lead-free solders, although some minor amendments of the proven procedures may be necessary e.g. a different etch for the lead-free microsections. Other salient points are:

- The ***micro-sectioning*** method has been shown to be the most suitable method to identify and locate cracks and to study changes in microstructure after thermal cycling. Although this method can encounter problems in locating cracks in small component solder joints, this disadvantage can be offset by examining the microsections in an SEM rather than in an optical microscope. The method is suitable for qualitative analysis of solder joints throughout their life-time

- The ***dye penetration*** technique has been shown to have advantages in quantitative analysis of solder joint cracks, and can be used to analyze the whole area of a crack. It is not dependent on the positioning of the cross-sectional plane as is the case with micro-sectioning.

- ***Shear testing*** is an established method for evaluating not only the degree of crack propagation and damage to the solder joint, but also the strength of the joint [2].

- By contrast, other mechanical tests (***pull test, 3-point and 4-point bend tests***) turned out to be highly technique dependent (the results depending strongly on the skills of an operator), or themselves induced further damage during the test. As a result, the tests produced non-consistent and invalid results. These techniques are regarded as immature and require further development before wider use.

- The results of thermal transfer testing showed that the size of the crack does not affect the ***thermal conductivity*** of the solder joint, until the crack is larger than ~70% of the termination length. Solder joints with cracks on such a scale would have already failed mechanically. Hence this method is unsuited to studying crack propagation, and this was confirmed by FEA modelling which showed no significant changes in the dynamics of the heat transfer through cracked and uncracked solder joints.

- Other techniques currently under development and not used in this study (e.g. real time X-ray, inductive or ultrasonic imaging) might be of value in the future, when their limitations in terms of spatial resolution have been addressed. Other techniques, such as those based on noise and surface roughness, are still only laboratory instruments.

- The work has demonstrated the value of FEA analyses in helping to assess the suitability of the measurement techniques studied, in particular by highlighting potentially important factors, and by helping to explain the results of practical tests.

9. Acknowledgements

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