

Arbitrary Waveform Synthesis using Binary Josephson Arrays

Peter Kleinschmidt^a, Pravin Patel^a, Jonathan Williams^a, Jan-Theodoor Janssen^a, Ralf Behr^b,
Johannes Kohlmann^b, Jürgen Niemeyer^b, Juha Hassel^c and Heikki Seppä^c

^aNational Physical Laboratory

^bPhysikalisch-Technische Bundesanstalt

^cVTT Automation/Measurement Technology

1. Abstract

The Josephson primary DC voltage standard is a very successful quantum standard. Recently it has become possible to divide Josephson arrays up into binary segments, thereby creating the possibility of developing a “digital to analogue converter” with quantum accuracy. These new arrays are based upon non-hysteretic Josephson junctions, which allow the voltage to be changed almost instantaneously.

In this paper we will investigate the properties of two different types of Josephson arrays, one type is an intrinsically shunted array of junctions or so-called SINIS array, while the second type is externally shunted via small on-chip resistors. The arrays are biased using a purpose built computer controlled bias source discussed in a separate paper in this conference. We will discuss the accuracy of the generated voltage and investigate the ac properties.

2. Introduction

A Josephson junction which is irradiated with microwaves of frequency f exhibits constant voltage steps (so-called Shapiro steps) at voltages $V = nf/K_J$ (n is an integer number and $K_J = 2e/h = 483597.9$ GHz/V) in its current-voltage (I-V) characteristic. In a Josephson DC voltage standard several thousand of these junctions are connected in series. The junctions in these arrays consist of a superconductor-insulator-superconductor (SIS) sandwich (e.g. Nb AlO_x Nb) and are designed to have a relatively large capacitance and a large quasiparticle resistance, which leads to a highly hysteretic I-V characteristic with zero-crossing voltage steps. It is therefore not necessary to bias each junction individually. These arrays are typically operated at frequencies between 70 and 90 GHz, and with about 15000 junctions any dc voltage up to about ± 10 V can be generated [1]. The voltage generated by these arrays is truly quantized because there are no stable states between steps. However, current noise can induce transitions between overlapping steps. Also, step selection is relatively slow and the array does not always settle on the same step.

For applications such as the characterisation of A/D and D/A converters and for example the Moving-Coil Watt experiment, a voltage standard, which can be programmed to a certain voltage fast and reliably, would be desirable. Such a programmable standard would also be capable of generating ac waveforms with a calculable rms value. The programmable Josephson standard was first proposed and realized by Hamilton et al. [2] and uses junctions with a non-hysteretic I-V characteristic. Due to this single-valued I-V characteristic, the junctions can be set to the desired voltage step virtually instantaneously. They are arranged in segments, which form a binary sequence, and each segment is biased individually. The overall voltage is the sum of the voltages generated by the individual segments. The junctions can be resistively shunted SIS, intrinsically shunted superconductor-normal conductor-superconductor (SNS) or SINIS junctions.

In this paper we report on measurements on a SINIS array fabricated at PTB [3] and a resistively shunted SIS array fabricated at VTT [4] using a bias source developed at NPL.

3. Binary Josephson Bias Source

Details of the bias source used for the measurements below are described in a separate paper [5], so we only give a brief summary of its capabilities here. The bias source can generate up to 15 separate bias currents, each set individually by a 12-bit DAC. The current range can be set as required, but is typically 50 mA with a 50 Ω output impedance. The rise-time in response to a step change is about 200 ns. The output noise is approximately 1 μA_{rms} in a 1MHz bandwidth. All the DACs can be latched simultaneously and the source incorporates logic for storing and reproducing a sequence of DAC settings for generating waveforms.

4. Measurements of a SINIS array

A SINIS array consisting of about 8192 junctions, divided into segments of about 4096, 2048, 1024, 512, 256 and 256 junctions was characterized using the bias source described above. Figure 1 shows the IV characteristic of the whole array and of individual segments. All segments were shown to be working. The $n = \pm 1$ step appears at a current $I_S = \pm 1.2$ mA for each segment. The number m of working junctions in each segment was determined by biasing the segment on the $n = 1$ step (applying I_S and microwaves of frequency f) and measuring the voltage V across it using a digital voltmeter. The number of working junctions is then simply given by $m = K_j V / f$. This measurement showed one of the junctions of the array to be shorted, resulting in 8191 working junctions (with the short in the largest segment). While this superconducting short in the largest segment changes the output voltage of the array at a given frequency, it does not prevent the array from being used as a programmable voltage standard (however, the junction failure limits a binary build-up, a useful self-check for a binary array, to the smaller segments).

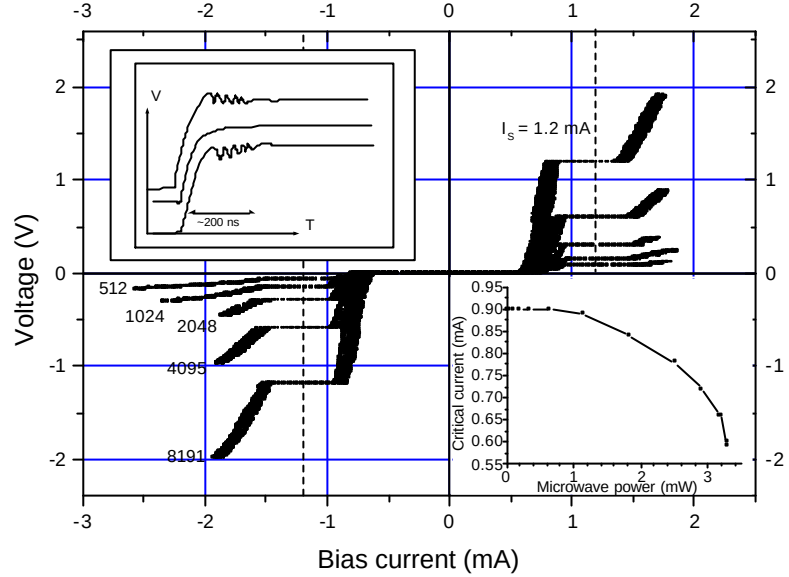


Figure 1: I-V characteristic of SINIS array (serial number BE-1/12; 3.3 mW microwave power at 70.084 GHz). Lower right inset: critical current as a function of microwave power. Upper left inset: Time response as observed on scope screen

The critical current of the array was measured as a function of the applied microwave power (see inset in figure 1). Without microwaves it is about 900 μ A, and with increasing microwave power it decreases to about 600 μ A at the largest microwave power available (3.3 mW, due to a lossy waveguide in the probe). The step width of $n = 1$ of the whole array was also measured as a function of microwave power. It increases smoothly with increasing power up to 500 μ A. However, the available power coupled into the array is insufficient to reach the maximum step width. In measurements of the same array carried out at PTB, the maximum step width was reached at about 14 mW microwave power.

Standard SIS arrays are used at zero bias current, and their voltage steps are truly quantized. This does not apply to programmable arrays, which are used at non-zero bias current and have a non-hysteretic I-V characteristic. It is therefore important to determine the required bias current for reaching the centre of the voltage step and to establish the flatness of the voltage steps under the conditions applied, as noise coupled into the array can result in sloped steps. The latter measurement can be carried out by comparison with a standard SIS array, biasing both arrays for similar output voltages

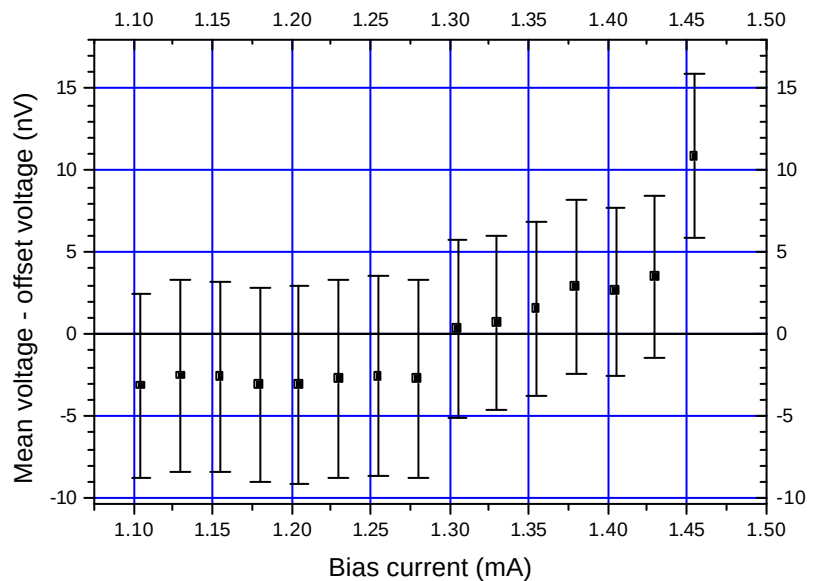


Figure 2: $n = 1$ step of SINIS array (average of about 10 sweeps), microwave power 3.3 mW at 70.084 GHz.

and measuring the voltage difference using a nanovoltmeter. The bias current of the binary array can then be varied by a small amount and thus the step mapped out precisely. Alternatively, two halves of the binary array can be biased in the opposite direction (with the bias source supplying two independent bias currents) and the voltage across the array measured using a nanovoltmeter. By varying the bias current in one of the segments, the flatness of the voltage step can be explored. The measurements reported here were made using the second method. Due to the shorted junction, a voltage of about 150 μV resulted, but by adjusting the offset of the nanovoltmeter, measurements at sub-microvolt level were possible. Figure 2 shows the result of one of these measurements. No filters were used in this measurement. Flatness of the step to within 10 nV over a bias current range of about 350 μA was established. Due to the connectors at the top of the probe (SMB), fluctuating thermal emfs prevented measurements with higher precision. An improved probe design is required to reduce these emfs.

Generation of ac waveforms is accomplished by programming the bias source to switch between different bias current settings. This results in an ac waveform consisting of a sequence of array voltages. The accuracy of the ac waveform generated by a programmable array depends on the speed of the transition between quantized voltage levels. In order to determine the suitability of the set-up for ac waveform generation, the response of the array to a step change in the bias current was investigated. The bias current was switched between zero and the current required for the centre of the $n = 1$ step. In this situation the output voltage changed smoothly from 0 to the $n = 1$ value during this step change without any overshoot (Figure 1, upper left inset, middle curve). However, switching to a current which was at the edge of the voltage step, resulted in a distinct ($\approx 5\%$ of amplitude) ringing in the output voltage, with the sign of the ring negative (positive) when switching to lower (upper) side of the step (Figure 1, upper left inset, lower (upper) curve). This demonstrates that the array “absorbs” the bias current noise when it is in a quantized state. The transition time was about 200 ns.

5. Measurements of a shunted SIS array

A shunted SIS array consisting of 3488 junctions was characterized in the same way as the SINIS array. When measuring the I-V characteristic of the array, voltage steps up to $n=3$ were observed. All segments and all junctions of this array were shown to be working. Figure 3 shows the IV characteristics of the whole array as well as of the individual segments (1744, 872, 436, 218 and 218 junctions). The characteristics show some hysteresis. Interestingly, the position of the steps in the characteristics seems to change to smaller bias currents for larger segments. This could be due to non-linearity of the current source or a reduction of microwave power present at the biased junctions when only part of the array is biased, which might affect the dc bias conditions.

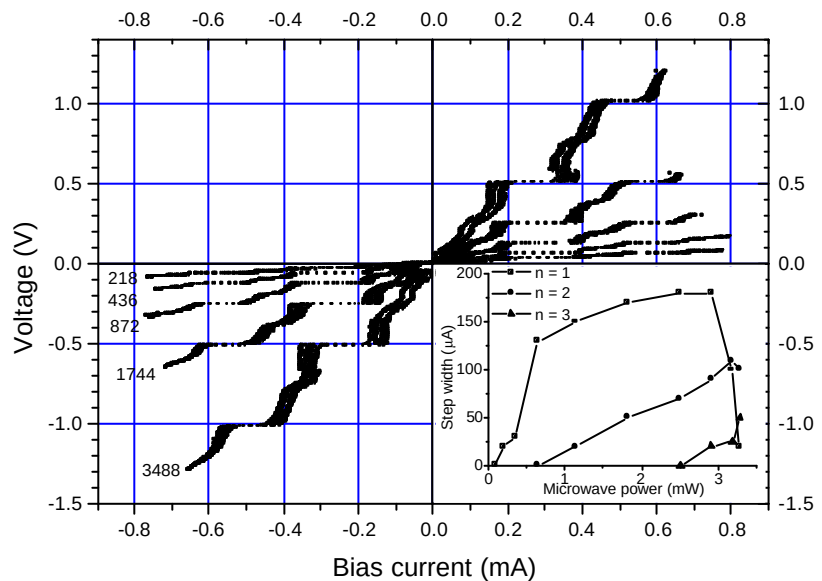


Figure 3: I-V characteristic of resistively shunted SIS array (serial number PV#22G5; microwave power 2.7 mW at 70.084 GHz). Inset: step width as a function of microwave power.

The critical current of $\approx 200 \mu\text{A}$ was measured without microwaves applied and decreases all the way to zero at 2.6 mW microwave power and above. The step widths of the $n = 1$, $n = 2$ and $n = 3$ steps were also measured as a function of microwave power (see inset in figure 3). With the $n = 1$ and $n = 2$ steps maxima were observed (at different power levels), while the $n = 3$ step did not reach a maximum within the microwave power available. At the highest power available the step width of $n = 2$ exceeded that of $n = 1$.

As with the SINIS array, precision measurements were carried out by biasing two halves of the array in the

opposite direction using two current sources and measuring the voltage across the array using a nanovoltmeter. One of the bias currents was varied over a narrow range and thus the step of the corresponding segment mapped. These measurements showed that without filtering the steps were in fact sloped, with a voltage change of several tens of microvolts. Filtering of the voltage leads using ferrite beads (approximately 140 μ H at 1 kHz) and a 220 pF capacitor and of the current leads using pi-filters improved the plateaux, though a slope of about 10 μ V was still observed.

Finally, the response of the array to a step change in the bias current was investigated (figure 4 and 5). There was no observable difference between switching the bias current from the centre of one voltage step to another and switching the bias current such that the step was not reached. This applies to measurement with, as well as without filters. As expected, there was strong degradation in the time constant of the response of the array to switching the bias current when filtering was used (from 200 ns to several μ s, with the pi-filters only).

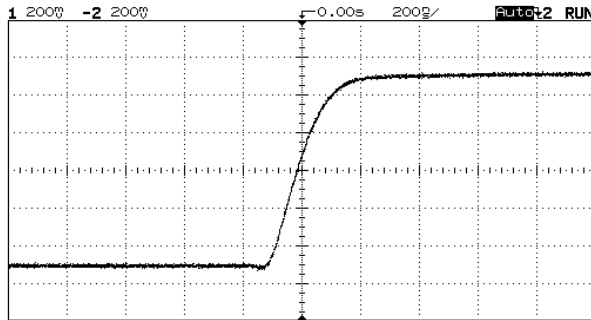


Figure 4: Response of resistively shunted SIS array to change in bias from $n = 1$ to $n = -1$ (no filtering, scale 200 ns/division)

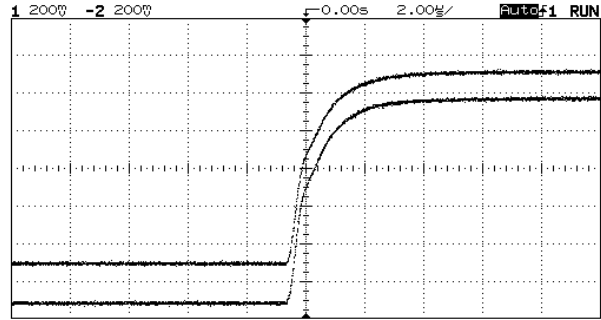


Figure 5: Response of resistively shunted SIS array to change in bias, top trace between centres of $n = -1$ and $n = 1$ step, bottom trace between two non-quantized levels.

6. Conclusion

Two binary Josephson arrays have been characterized using a purpose-built bias source. In order to obtain a programmable Josephson standard and to generate calculable ac waveforms, further progress in the following areas is required: Flatness of the voltage steps to sub-nanovolt level has to be established. In the case of the shunted SIS array, improvements to the noise level of the bias source and/or the noise sensitivity of the array are necessary. The combination of the bias source with the SINIS array seems suitable for a programmable Josephson standard without any modifications, but a more accurate measurement of the voltage steps with elimination of thermal emf fluctuations has to be carried out. Ideally, filtering should be avoided as it degrades the switching speed of the source. Generation of ac waveforms will then be possible and the accuracy of the rms value of the resulting waveforms can be checked using thermal voltage converters.

7. Acknowledgement

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8. References

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