

A Programmable Bias Source for Binary Josephson Junction Arrays

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1. Abstract

A bias source has been designed and constructed for use with a new generation of so-called binary Josephson junction arrays (JJA). Each segment or bit of this JJA has to be biased individually. The design consists of a motherboard on which up to fifteen separate bias sources can be plugged in. Each bias source is a fast (200 ns settling time) programmable precision current source in a screened enclosure. An optical interface provides electrical isolation of the source from the controlling computer. Waveform data can be loaded into memory and played back to produce the desired waveform. In this paper we will discuss the electronic design and report on the performance specifications.

2. Introduction

During the last few years binary Josephson arrays have become available. The principle and characteristics of these arrays are discussed in a separate paper at this conference [1]. The arrays are made up of a large number of Josephson junctions, divided into segments in a binary fashion. Each segment or bit of this array has to be biased individually. The concept for generating AC Josephson voltage waveforms using arrays of this type was first developed by Hamilton et al [2]. When using a binary array to generate an ac waveform the accuracy of the waveform depends on the transition time between different voltage levels which should be as short as possible. In this paper we discuss the development of a fast bias source for these arrays with rise time of the order of 200 ns.

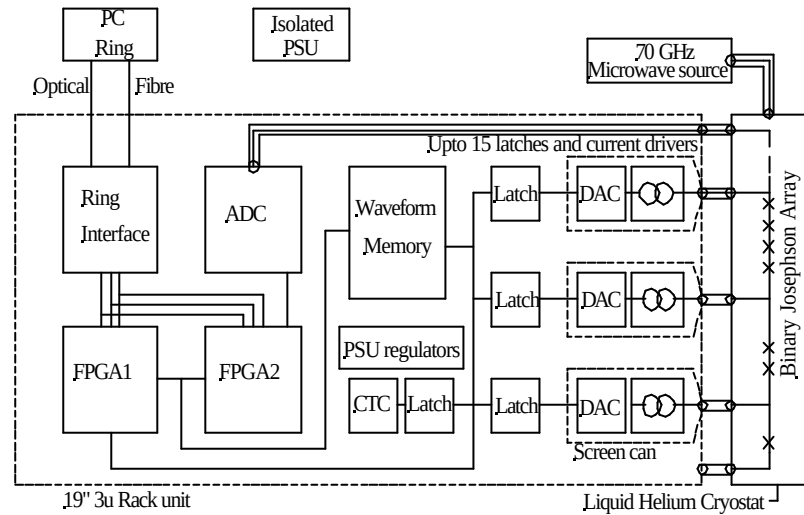


Figure 1 Block diagram of bias source

3. Concept

A block diagram of the bias source is shown in figure 1 with the digital functions on the left hand side and the analogue circuits for driving the array segments on the right hand side. The bias source is connected to a PC using an optical fibre ring computer interface [4]. This interface isolates the bias source from digital noise generated by the PC. The digital Field Programmable Gate Arrays (FPGA) controls the flow of digital data between the computer interface, waveform memory and data latches. There are a total of 15 locations for the analogue bias current drivers; each with its own data latch and the bias source configuration can be changed by substituting different current source modules. This allows the bias source to be optimised for different types of binary array. In order to generate a periodic arbitrary waveform, the bias source stores up to 32 kbyte blocks of data. Each block contains the bias current settings for the 15 array segment bias drivers at a particular point on the waveform plus a delay parameter which determines the time between the present point and the next.

3. Bias current driver circuit

In order to obtain the desired switching speed for the array, it is necessary to have sufficient drive capacity in the bias source to charge the coaxial cables which connect the array to the bias source. A 50 Ω design has been chosen so that their characteristic impedance drives the coaxial cables. This in turn means that to reach

approximately 5 V, a drive current of ± 100 mA is required.

The combination of voltage, current and speed was found to be outside the range of operational amplifier performance so a design using discrete components was developed. This is based on an earlier precision current source produced for cryogenic current comparator work [3]. A simplified diagram of the current source is shown in figure 2. An FET input stage (Q1 & Q2) form a long-tailed pair differential amplifier with the tail resistor replaced by a constant current source (Q3) to improve the common mode rejection ratio. The FETs provide the high input impedance, so as not to load the input potential divider formed by R1 and R2. The outputs from the first stage are fed to a differential input intermediate stage (Q4 and Q5) before the final output stage formed by Q6 and Q7. Current feedback is via R10. In order to obtain a bipolar drive, the circuit is repeated with the opposite polarity and the two currents combined at the output terminal to the array segment.

The current source is fed from a voltage generated by a fast 12 bit bipolar Digital to Analogue Converter and associated amplifier (IC1 and IC2). Figure 3 shows the complete current driver housed in a screening can to reduce cross talk between drivers. The current driver operates in class A bias with a quiescent current of 60 mA. This leads to a power dissipation of about 2 W so the screening cans are also used as heat sinks for the output transistors. The use of precision surface mount components leads to a small overall size of the plug in modules.

4. Digital drive electronics

The digital control section consists of the optical fibre ring interface, memory interface, select control, timing control, and a 16-bit DAC interface. Although the present design uses a 12-bit DAC, the digital circuit has the capacity to accommodate a 16-bit device. Most of the digital design is done in the

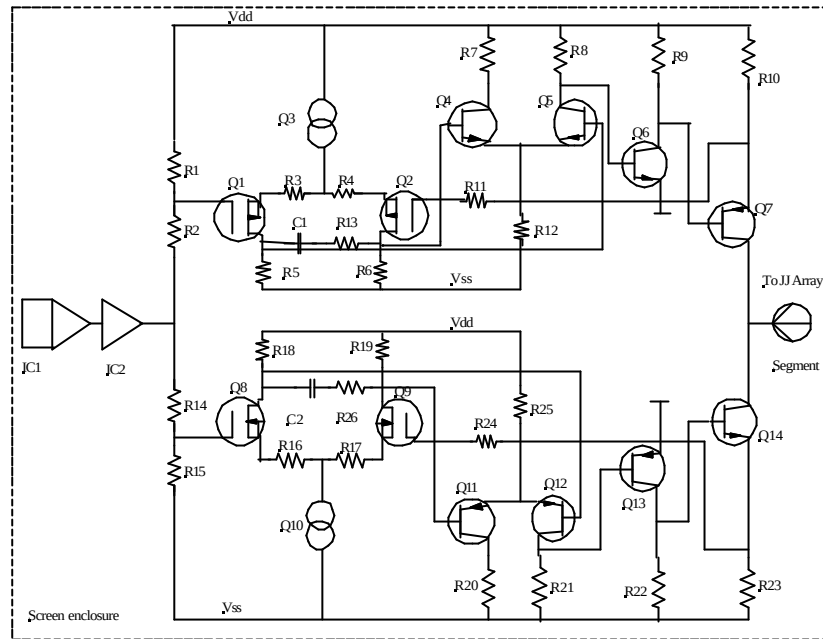


Figure 2 Schematic diagram of the current source

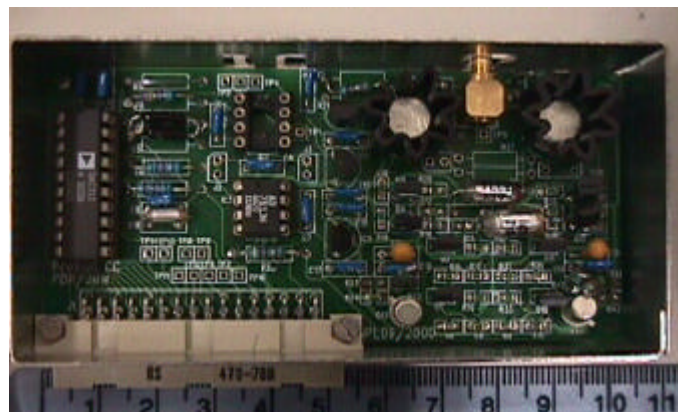


Figure 3 Current source PCB

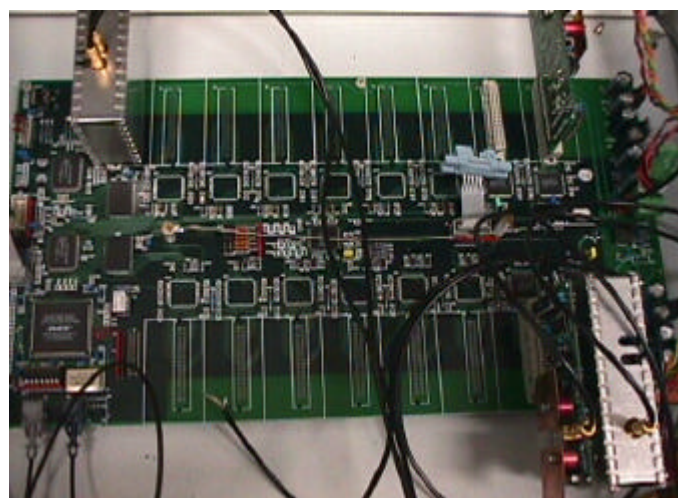


Figure 4 Complete bias source

FPGAs which can be programmed or erased whilst on the board via the parallel interface of the PC. The 16-bit wide data bus is common to all 15 data latches and the Counter-Timer Chip (CTC programmable delay generator).

The digital electronics has two modes of operation. In the PROGRAM mode, FPGA1 is active and part of FPGA 2 is disabled. The controlling computer can access the waveform memory and write directly to the DACs. This allows the individual I/V characteristics of the array segments to be explored and the bias points for waveform generation found. In the RUN mode, data blocks from the waveform memory are transferred to all 15 holding latches sequentially followed by data for the CTC. Each data block consists of fifteen 16-bit words, one for each bias driver and a single 16-bit word which contains the delay data for the CTC. The data blocks repeat every 16 memory locations. Each word transfer takes 100 ns and once the CTC is loaded, the delay period starts. After the delay period all the holding latches transfer their data simultaneously to their DACs and the next sequential transfer begins. In this mode the disabled part of FPGA 2 is active and takes over the address bus from FPGA 1. FPGA 2 generates the addressing sequence required to replay the stored waveform using its 24-bit address counter. Figure 5 demonstrates the capability of the system. This trace is the output from a single channel of the bias source where the DAC and delay values have been calculated to produce a staircase approximation to a sine wave. Figure 6 shows an arbitrary waveform generated by a single channel of the source.

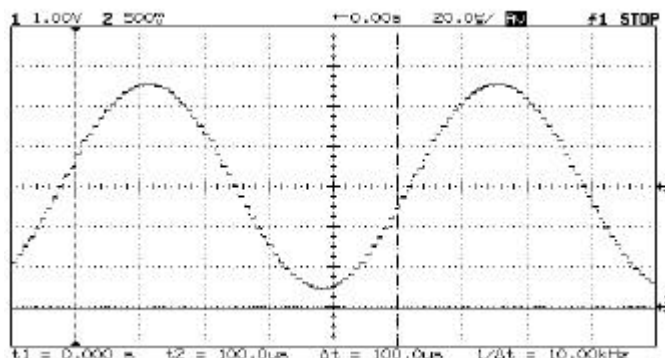


Figure 5 Sine-wave synthesised by one channel

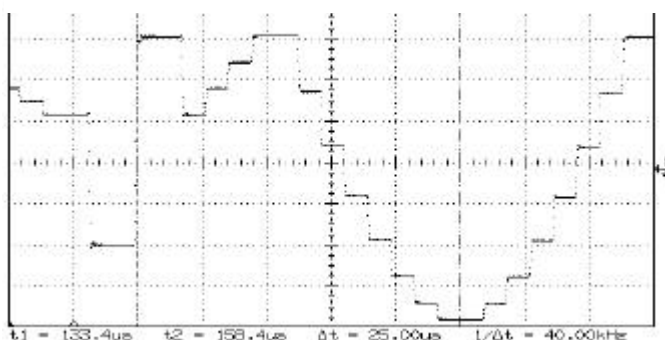


Figure 6 Arbitrary waveform synthesised by one channel

A 22-bit effective Analogue to Digital Converter (ADC) is also incorporated into the design. This is used to measure the segment I/V characteristics and to digitise the AC waveform in the RUN mode. Sampling successive points digitises the AC waveform. The digital circuit using an address comparator generates the timing for this process.

The complete bias source is shown in figure 4 and is housed in a standard 3U Euro rack. On the lower right hand side is a bias driver in its screened box and on the top left hand side is the ADC unit. Two further bias drivers without their enclosures can also be seen.

5. Characteristics of the bias source on JJA

Figure 7 shows small signal response with a 50 Ω load. A small amount of ringing can be seen on the top of the trace. Figure 8 shows the transition from $n = -1$ to $n = 1$ on a single segment of an SIS array. It can be seen that the desired rise time of 200 ns is being achieved. The current noise from the bias source has been separately measured and found to be 1 μA in a 100 kHz bandwidth.

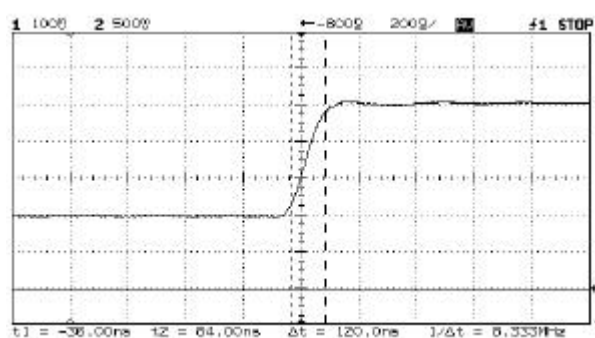


Figure 7 Small signal response

6. Conclusions

A fast programmable bias source for the new generation of Josephson junction arrays has been constructed with the capacity to drive binary arrays with up to 15 bits. The bias source has achieved a 200 ns rise time on an array segment. Further work needs to be done to reduce the current noise on the output, and the small drift seen at the output due to the high power dissipation of the drivers. In addition an improved sample and hold is needed at the input end of the ADC. The bias source can be used both to measure the I/V characteristics of the array and to generate the bias signals required for waveform synthesis.

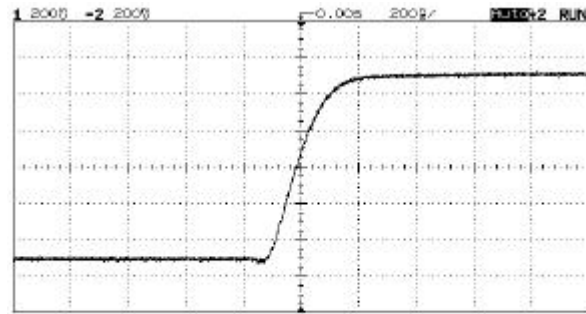


Figure 8 Step transition on an array

7. Acknowledgements

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8. References

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