

An AC Voltage Standards Based on a 1-Bit Current Steering DAC

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1 Introduction

This paper describes the development of an ac voltage standard based on a 1-bit current steering DAC. The standard gives a 10 V rms output with an uncertainty of $\pm 1 \mu\text{V/V}$ up to about 300 Hz. The theory and design of the standard is described and some results and uncertainties are presented.

2 The Synthesis of Waveforms

A sinewave can be synthesized by feeding a suitable digital sequence to a DAC. The resulting DAC output is a piece-wise approximation to the sinewave (a sinewave made up by steps). The DAC output is then filtered to remove the sampling harmonics giving a smooth sinewave. Assuming the data to be correct, the accuracy and distortion of the resulting sinewave is determined by the properties of the DAC namely the resolution, the number of steps used to construct the waveform [1], the accuracy of conversion, the linearity, the value of the dc reference and the characteristics of the filter.

3 The Principle of a 1-Bit DAC

It is possible to make a highly linear DAC using just one pair of switches. Such a system is shown in Figure 1. The operation of the switches is such that the pulsed output shown in Figure 1 is produced. The dc value of the filtered output is defined by the mark-space ratio of the switched waveform. If the mark space ratio is modulated by digital data appropriate for a sinewave and if the filter is properly designed the output will be the required sinewave.

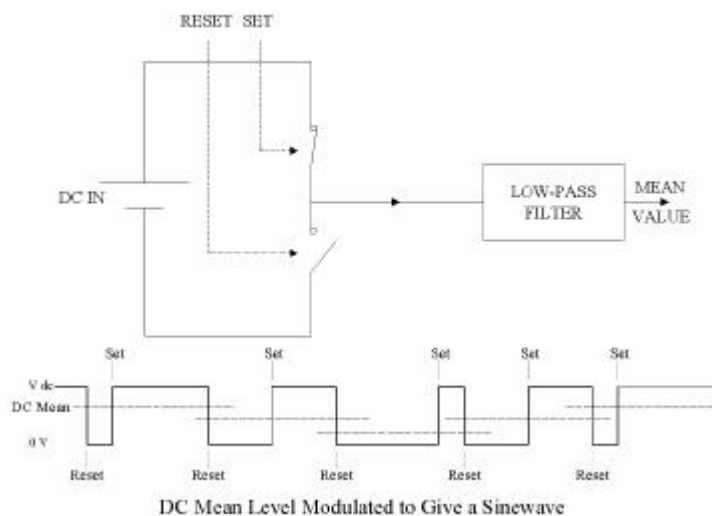


Figure 1, 1-Bit DAC Principle

The system has a number of advantages over the conventional multiplying DACs. The use of just one switch pair reduces the scope for switch errors and also allows the designer to concentrate considerable effort into the operation of this pair of switches rather than having to deal with the many switches contained in other DAC designs. The path from the dc standard to the ac output is relatively simple, leading to better traceability.

To define the On/Off times a fast clock is used with electronic counters to give timing resolution. The NPL design uses a scheme which is independent of timing errors in the counters [2], leading to a highly linear system (better than $\pm 1 \mu\text{V/V}$). The switches are field effect transistors which introduce errors due to charge injection where the gate pulse used for switching couples into the drain-source channel. Timing edges must be very well defined and jitter kept to an acceptable level.

The resolution of the DAC is set by the switch timing resolution. If the logic that defines the timing is operated at 52 MHz (a practical limit), the timing for synthesising a 50 Hz sinewave can be resolved to 9-bits.

The initial work on an ac standard was based on a voltage switching DAC [3] this was recently re-worked using a design that incorporates a field programmable gate array (FPGA). This has the advantage of condensing fast and hence potentially noisy digital electronics into a single chip. Using this approach it was possible to dispense with the separate digital driver unit which had been previously isolated by optical fibres, and replace it with a single chip with very short load paths to the analogue switches that make-up the DAC. This led to a compact and more reliable design with improved noise performance.

4 Current Steering DAC

Whilst voltage steering is conceptually simple, advantage can be had by use of a current steering design for the 1-bit DAC.

In this approach the dc input voltage to the DAC is converted to a current using a voltage to current converter circuit. To make the pulse width modulated (PWM) waveform, the current is either steered to ground (the off state) or to the input of a current to voltage converter (the on-state). The voltage is then filtered as in the voltage switching case.

This approach has the obvious disadvantage that the system requires two extra conversion stages which require characterisation. The current steering operation of the analogue switches does however give significant advantages. As the current source resistance feeding the switches is very high, the on-resistance of the switches is not a significant problem, which allows the use of small geometry transistors which have lower capacitance. Further the junction capacitance of the switches is not modulated as the switches work at a constant potential. With one terminal at ground level, the configuration is readily guarded.

5 System Design

In a departure from previous designs it was decided to work at a 10 V dc input level, rather than 1 V. This gives noise advantages at the expense of some design and component selection problems.

It was also decided to make a bi-polar system, which requires a difficult balance in the two halves of the circuit but gives improved dynamic range and avoids dc offset problems at the output.

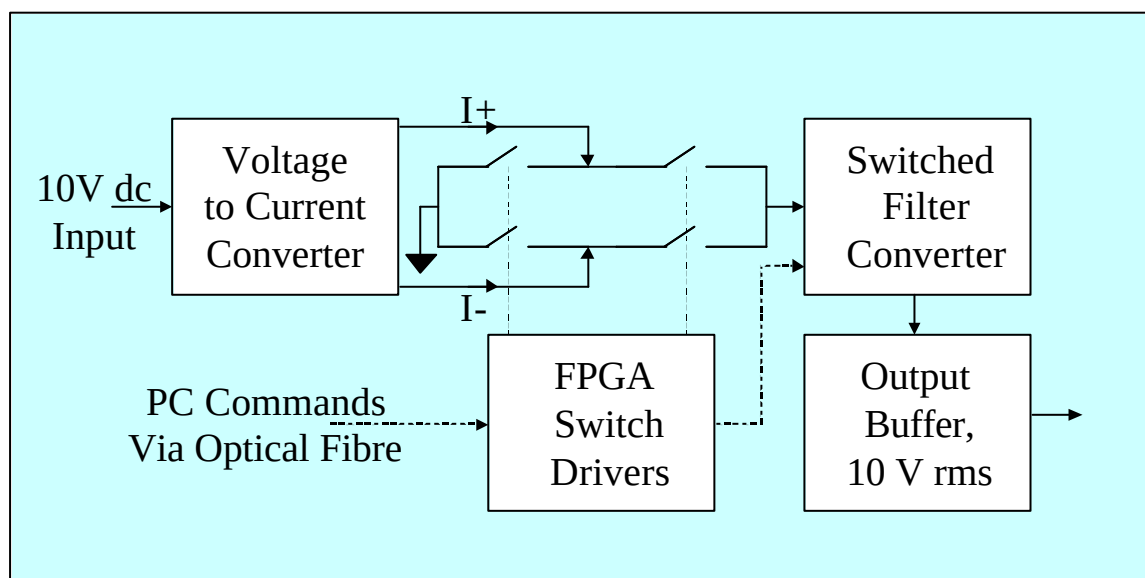


Figure 2, Schematic of Current Steering DAC AC voltage Standard

A schematic of the system is shown in Figure 2. DMOS switches alternately steer the positive and negative currents to the output converter stage, the unused polarity being steered to earth. The PWM control of the switches is achieved using the FPGA logic circuits of a similar design to that used in the voltage DAC system.

The Voltage to Current converter circuit consists of a resistor and two precision current mirrors which source the currents of both polarities. To overcome the significant problem of accurate V to I and I to V conversion, a single resistor network was used to perform both V to I and I to V conversion. This is shown in Figure 3.

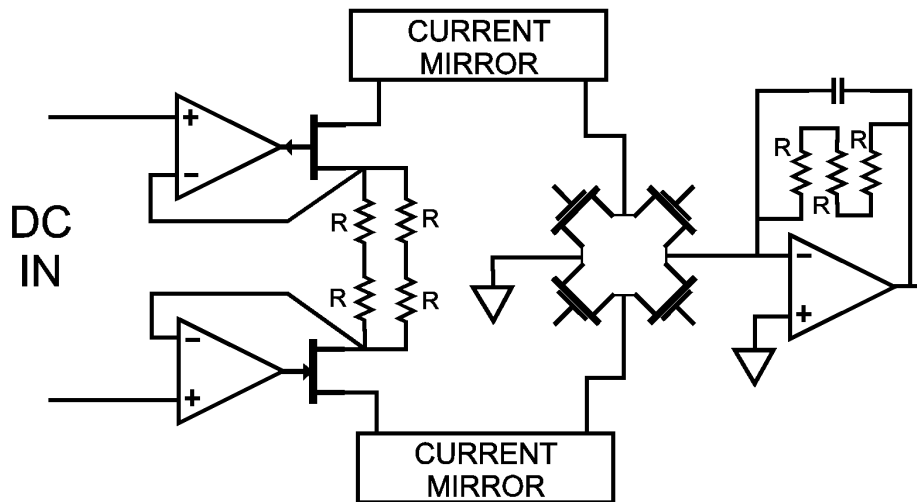


Figure 3, the use of "statistical" average matched resistors in V to I and I to V conversion

The circuit has a gain of three, very accurately defined by the "statistical" average matching of the TaN film resistor elements (R), which are of equal value on the same substrate. The stability of this type of arrangement has been shown to be better than $0.1 \times 10^6/K$ and $0.5 \times 10^6/\text{year}$.

The V to I converter uses cascode output stages to provide a very "stiff" current source insensitive to the demanding voltage changes induced by the subsequent circuits.

The switching is so arranged that every DAC code consists of at least one pulse of current in each polarity,. For example the code +2 would consist of a positive pulse 3 time units long and a single time unit negative pulse. Similarly -2 would have a 3 time unit negative current pulse and a single time unit positive pulse. A zero code consists of a single pulse of each polarity. In this way the switching is balanced with both an equal number of switching edges per cycle for each polarity and also a constant number in total per unit time.

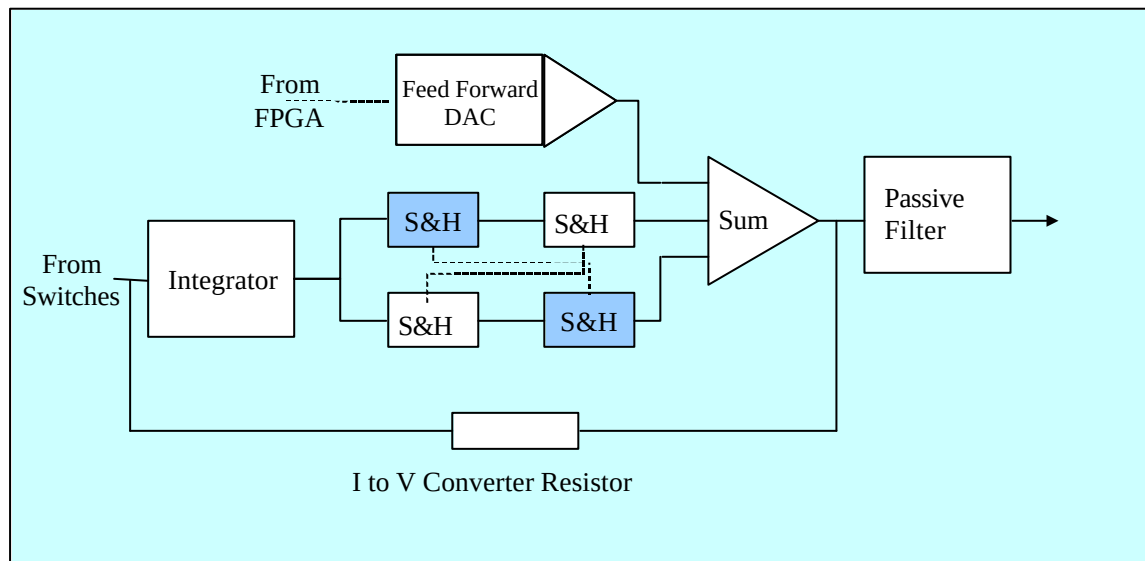


Figure 4, Switched Filter Converter Stage

I to V conversion and filtering is performed using the switched filter converter stage as shown in Figure 4. This stage consists of a fast integrator which includes the I to V TaN resistors in a feed back loop which define the LF gain. A switched filter uses a pair of sample and hold amplifiers to alternately sample the integrator output on

alternate DAC code periods. This is followed by a further pair of sample and hold amplifiers, these track during the hold period of the previous stage and hold during the track period. In this way the dynamic response of the integrator within each DAC code period is rejected.

Performance is improved by limiting the voltage across the sample and hold capacitors to reduce dielectric storage effects. This is achieved by using a DAC to feed forward an approximation of the desired output value at each DAC code period. In this way the integrator only needs to charge the capacitors sufficiently to make the small correction between the predicted value and desired magnitude.

Any remaining switching spikes are removed by use of a passive output filter which, as a result of the switching filter, no longer needs to have so precisely defined components. This output is then fed to an output source and sense buffer stage.

6 Results and Uncertainties

In order to calculate the ac voltage value of the standard it is necessary to measure the gains of the various stages in the system. This is carried out using automated measurements using two digital voltmeters which can be reversed in order to cancel errors. The measurement of the gain and the spread of the results is a major contribution to the uncertainty and it is difficult to achieve much better than ± 1 ppm using this method. The stability of the various system gains has stayed within this ± 1 ppm over a period of 8 months.

Issues such as aperture error and quantization errors are also considered; these are discussed in more detail in [3]. Other possible errors include switching glitch errors and charge injection; as there is no noticeable deterioration in the performance in the system at higher frequencies, this backs-up the theoretical predication that these errors are insignificant at 50 Hz in this design.

Regular measurements have been made using a Wavetek 4920 electronic ac/dc transfer standard. Transfer was made against the dc reference used to supply the 10 V input to the ac standard. Transfer measurements on the ac standard were made using the 4920 over a range of 76 Hz to 305 Hz. The mean transfer value of these measurements was found to be $+4 \mu\text{V/V}$ (the ac standard is high). This value is within the estimated ac/dc difference uncertainty of the 4920 of $\pm 12 \mu\text{V/V}$ (95% confidence). The transfer value shows no detectable frequency dependence up to 305 Hz, although there is a $15 \mu\text{V/V}$ increase in value at 381 Hz.

7 Conclusions

An ac voltage standard using a 1 bit current steering DAC has been constructed. The standard converts a 10 V dc standard input to an ac 10 V rms output at low frequencies. The uncertainty of the calculated ac value is dominated by the measurement uncertainties of the system gain measurements, giving an estimated uncertainty of $\pm 1 \mu\text{V/V}$.

A number of issues remain to be resolved, such as increasing the frequency range of the device. There are a number of desirable circuit improvements which could be carried-out to improve performance. A theoretical scheme for increasing the resolution of the DAC to 24 bits could be developed in a future version.

8 Acknowledgements

The development of the ac voltage standard as described in this paper was supported by the DTI National Measurement System Policy Unit's Programme for Electrical Metrology.

9 References

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