

TOWARDS CALIBRATION OF IVDs UP TO 1 MHz USING PERMUTING CAPACITORS METHOD

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Abstract

A device which employs the permuting capacitors method for calibrating inductive voltage dividers (IVDs) has been fabricated. Eleven nominally equal 5 nF capacitors, having NPO ceramic as the dielectric, form the core of the device. A compact design, which is important for high frequency measurements, was realised using printed circuit-board fabrication. The eleven capacitors are fully shielded to reduce errors from stray capacitances.

Introduction

At present there is a lack of traceability for many commercial instruments which claim to be able to measure impedance up to a few MHz with an accuracy better than 0.5 %. To bridge this traceability gap between the low frequency region (typically 1-10 kHz) and the higher frequency region of up to 1 MHz, an array of components have been fabricated to assemble a high frequency four terminal-pair bridge [1]. These components are decade value resistance and capacitance standards, high frequency IVDs, isolation transformers, and a 'permuting capacitors' device (PCD). The latter is needed for a well known technique of permuting eleven nominally equal value capacitors in a bridge to determine the ratio error of an IVD at a given setting and excitation frequency [2,3]. To determine the frequency dependence of the impedance standards as accurately as possible, all sources of errors and their frequency dependences when incorporated in a bridge system must be investigated so that these errors can either be eliminated or if that is not possible then included in the uncertainty budget. Three of the main sources of the many errors in an impedance bridge are associated with the standards, high frequency IVDs and the connection cables. To characterise the standards accurately, the last two sources of errors must be eliminated to a sufficient level to meet the desired overall accuracy. Error contributions from cables are kept small by using short lengths and by making a calculated correction [3]. More importantly, the error contribution of the high frequency IVDs can be measured by the permuting capacitors technique where the basic principle idea is shown in Fig. 1. An error which can occur in this technique arises from the voltage dependence of the capacitors as the capacitors are *permuted* from the low to the high voltage arm of the bridge. This source of error can be eliminated by measuring their voltage dependence using gas-dielectric capacitors whose voltage dependence is negligible. The eleven capacitors of 5 nF nominal but closely matched values were made by connecting in series two 10 nF capacitors selected from a large batch. There are several benefits from using capacitors having an NPO ceramic dielectric, a small temperature coefficient of approximately $13 \times 10^{-6}/K$, dissipation factor of only about 7×10^{-5} , a small voltage coefficient, negligible

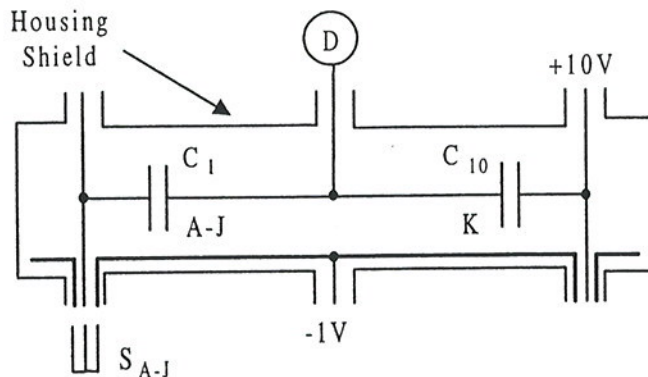


Fig. 1. Cross-section of the basic layout of the PCD, where A-K refers to capacitor numbers and S to a short. Shielding for the 'active' circuit areas are not shown.

capacitance hysteresis from temperature cycling and minimal residual self-inductance due to their small physical dimensions of $5.5\text{mm} \times 5\text{mm} \times 0.75\text{mm}$, permitting use for our purpose at frequencies up to at least 1 MHz [4].

Fabrication of the Permuting Capacitors Device

There is considerable benefit to be gained in a circular geometrical construction in that it ensures the near equivalence of each capacitor by making the parasitic impedances associated with each capacitor nearly identical, in addition to the ease of design and fabrication. Fig. 2 shows the series connection of two 10 nF NPO ceramic elements at each of the eleven segments. The twelfth segment shown at the 'nine o'clock' position is left blank, as it is used for the -1V connection from the IVD under test. It should be noted that each of the two 10 nF capacitance elements are connected in an unstressed manner by connecting a small loop of thin flexible copper foil (having low self-inductance) between them. The overall dimensions of the device board shown in Fig. 2 is $100\text{mm} \times 100\text{mm}$, and each segment has two PCB SMB sockets mounted on the reverse side of the board (forming an *inner* and an *outer* circle of connectors). The central connector is the detector terminal. The ten capacitors can be 'paralleled-up' by inserting a short at the outer circle of connectors - thus eliminating the use of cables, which at high frequency would limit the accuracy attainable using this method. To achieve the parallel connection of the ten capacitors, on the reverse side of the board is a thin copper plate which is connected to the SMB shields of all the eleven outer circle of connectors. Therefore by shorting the appropriate number of inners to outers of the SMB sockets various ratios of capacitance can be achieved. The inner circle of connectors have their shields connected to the overall device shield, to which the detector shield and the housing box are also connected.

The device must be tested for temperature stability of all the capacitors and their stability to the inevitable disturbance when a short is moved manually from one position to the next - which could produce mechanical disturbances as well as a short thermal pulse into the device. The overall temperature stability of all the capacitors connected in parallel (giving an average temperature dependence) has been measured to be within $\pm 1 \text{ ppm}$ over a 24 hour period. This is more than adequate since the bridge network (described below) used for calibration has a one *ppm* resolution. In

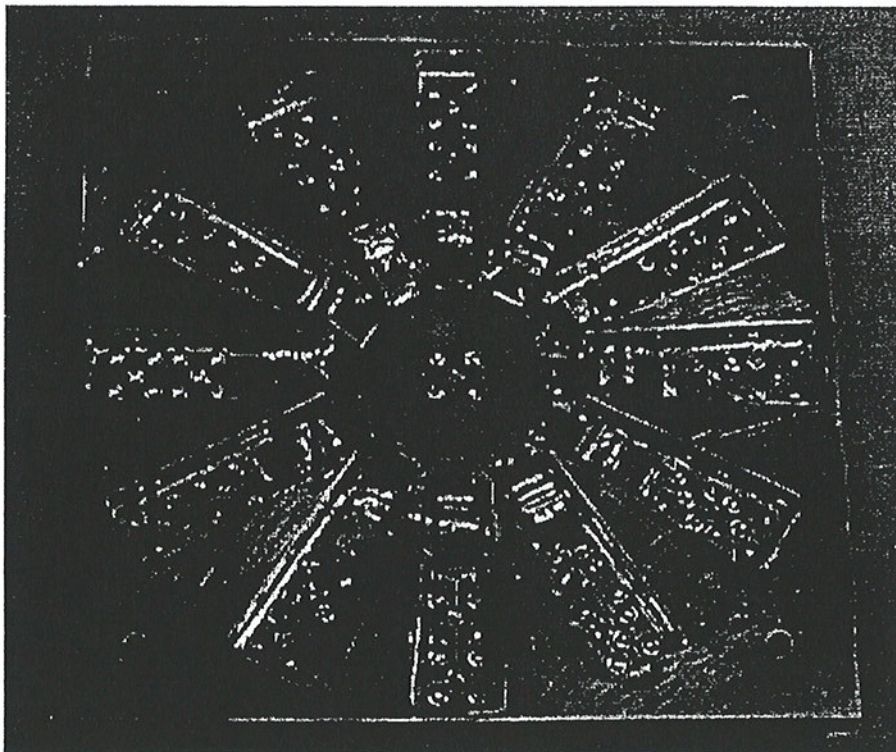


Fig. 2. PCB mounted eleven 5 nF NPO ceramic capacitors connected to the detector terminal in the centre of the PCD.

the initial design when a short was moved to another position, the thermal disturbance was such that it took almost four hours for the capacitance value to regain a steady value (the maximum shift was 10 ppm). Fig. 3 shows the results of a similar test after a copper plate was thermally coupled to all the SMB connectors but electrically isolated from them, to form a thermal anchor. The thermostating heating elements were also attached to this copper plate. There are three main points to note from Fig. 3. Firstly, it takes approximately three hours from when the thermostating circuit is activated for the device to reach a steady value, of approximately 25 ppm above the first measured data point. Secondly, the glitches seen from zero to 2.5 hours were interference from the mains operated 12V DC source. These were reduced to less than 1 ppm using a better source. Thirdly, and more importantly, the eleven jumps (corresponding to the eleven capacitors) in the last part of data are due to the shorts being disturbed. In contrast to the previous design, where such a disturbance took several hours to reach a steady value, here the return to the normal drift line is immediate - which shows also that there is negligible hysteresis.

Calibration Bridge

The bridge used for calibrating the test IVD using the PCD is shown in Fig. 4. It is essentially a two terminal-pair bridge converted to a four terminal-pair network by using T-connectors to form the separate current and potential defining points at the 'high' current and potential terminals. The bridge is balanced by injecting a small current via a small injection capacitor C_i connected to the output of an IVD which is driven from the same $\pm V$ output terminals of the isolation transformer. For a valid calibration the IVD under test must have its magnetising winding energised, as shown in Fig. 4. The bridge also employs a Wagner balance and current equalisers but the effectiveness of the latter diminishes beyond about 50 kHz. The balance equations as the eleven capacitors are permuted can be summarised as [3] :

$$(1-n) \sum_{i=1}^{r+s} Y_i + \Delta Y \sum_{i=1}^{r+s} k_i - n(r+s)\Delta Y = ns \sum_{i=1}^{r+s} Y_i \quad (1)$$

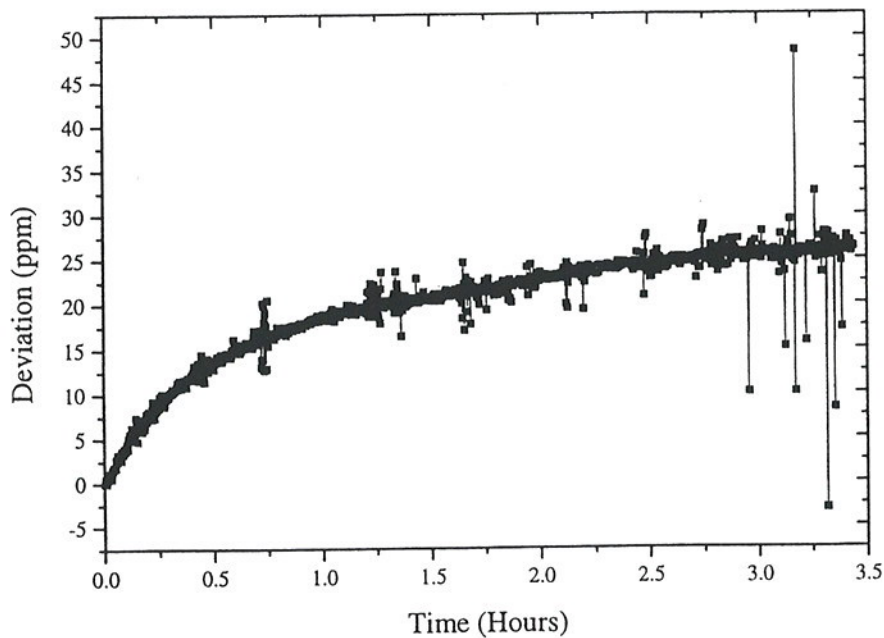


Fig. 3. Influence of ambient temperature on the stability of the PCD and user interference (near the three hours point).

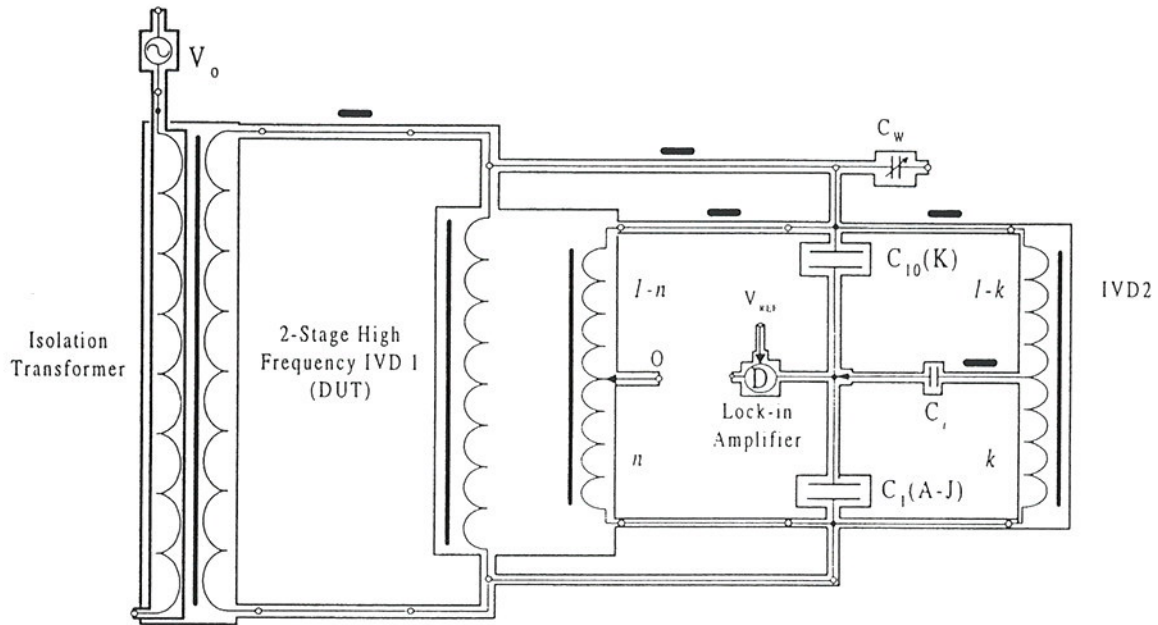


Fig. 4. Coaxial bridge for calibrating IVD 1 using permuting capacitors A-K.

where Y_i is the i -th value of the admittance being permuted, $r = 1$ and $s = 10$, n and k are the settings of the test and injection IVDs respectively. Equation (1) simplifies to :

$$\frac{1-n}{n} = s + \left(1 - \frac{\bar{k}}{n}\right)t \quad (2)$$

where $\bar{k}$ is the average value of the injection IVD settings, and t is the ratio of the injection admittance $\Delta Y = \omega C_i$ to the average admittance of the eleven capacitors. In the permuting capacitors method the variation in value of the individual capacitors with frequency is not needed, as can be seen from (2). However, it is worth noting that both $\bar{k}$ and t have finite frequency dependence, but it can be shown that neither contribute appreciable error, certainly for the accuracy sought.

Conclusions

A compact PCB based device for permuting capacitors has been fabricated to calibrate high frequency IVDs up to 1 MHz. Initial designs have been modified to obtain better stability to ambient temperature variations, and in particular, significant improvements have been to avoid disturbances resulting from manual permutation of the capacitors. Results will be presented showing comparisons with the standard NPL IVD calibration which uses the build-up technique.

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