

Optimum Pad Design and Solder Joint Shape for Reliability

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ABSTRACT:

This report contains the results of a NPL programme to develop test methods for assessing solder joint reliability by thermal fatigue and computer modelling of solder joint failure. The life-time of chip resistor solder joints under thermocycling load has been correlated with solder joint shape, solder volume and pad size. An electrical DC measurement method for assessing solder joint reliability was evaluated for a range of current temperatures. The robustness of the DC method for monitoring joint failure is considered, with voltage scans and in-situ measurements used to reveal the limitations of this technique.

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ISSN 1361-4061

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Approved on behalf of Managing Director, NPL, by Dr C Lea,
Head, Centre for Materials Measurement and Technology

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1. INTRODUCTION

The use of pad design guidelines is widespread in the electronics manufacturing industry, but with the ever increasing high levels of integration in modern assemblies there is considerable pressure to vary these preferred designs to squeeze more onto the PCA (printed circuit assembly). The effect of these changes on solder joint reliability is not well known. In this report we assess solder fillet geometries formed with different pad geometries and stencil thicknesses using SM (surface mount) resistors.

The reliability of a surface mount assembly is dependent on the service environment, the expected cyclic service life, and the acceptable cumulative failure probability at the end of the cyclic service life. The reliability of a surface mount component, also depends on the assembly design parameters such as size, shape and materials.

1.1 DESIGN

Design parameters identified to have a primary (first order of magnitude) influence on SM solder attachment fatigue reliability are:

- Component size

The physical size of the component determines the amount of displacement a solder joint experiences during thermal expansion/contraction. This is due to the different CTE (coefficient of thermal expansion) of the component and the substrate. Larger components have a greater impact on reliability.

- Solder joint area

The solder joint area determines the stress in a solder joint resulting from a given component/substrate displacement. It is of importance, primarily for compliant lead attachment. Larger solder joint areas reduce the applied stresses and increase reliability, however the magnitude of this effect is very small.

- Coefficient of Thermal Expansion

The linear coefficient of thermal expansion (CTE) represents the change in linear dimension of a material due to a change in its temperature. Components and substrates consist typically of a variety of materials all having different CTEs; the effective CTEs are a combination of the individual materials CTEs and are typically dependent on component and substrate orientation. CTEs need to be measured for both product and test vehicles to avoid possible large errors in the reliability predictions.

1.2 DAMAGE BY FATIGUE AND CREEP MECHANISMS

The cyclic nature of the temperature variation causes the strain experienced by the solder joints to be cyclic and, therefore, the damage in the solder to be a function of the number of thermal cycles. By this definition, SMT solder joints experience not only fatigue but thermal fatigue. At low temperatures (below $T=T_m/2$), fatigue can cause damage by the initiation and propagation of microcracks. T is operating temperature and T_m is melting temperature. The equation used to describe fatigue life N_f is the Coffin-Manson relation (1), generalised fatigue damage function:

$$N_f = C \left[\Delta \gamma_p \right]^{\frac{1}{c}} \quad (1)$$

where:

C is a material constant

c is in the range of -0.5 to -0.7 for most metals.
 γ_p is strain range

In general, surface mounted components see thermal cycling that can range from $0.4T_m$ to $0.75T_m$. Accordingly, it can be argued that in most microelectronics applications, the life of a component is spent at temperatures above $T=T_m/2$, which is about room temperature for the highest melting point SnPb solders. As a rule of thumb, creep is an operative deformation mechanism whenever the temperature is above $T_m/2$ [5].

2. EXPERIMENT

An experiment investigating the influence of land pattern pad designs on the reliability of solder joint attachments for chip resistors is described here. The assemblies were tested for ten months.

2.1 TEST ASSEMBLIES

Fifty four PCBs were manufactured for this experiment; 3 lots of 18 PCBs, with each lot being manufactured using a different stencil. Each PCB incorporates 35 0805 chip resistors and 35 2512 chip resistors. The nominal value of the 0805 resistors was $47\text{ k}\Omega$ and $1\text{ k}\Omega$ for the 2512 resistors. There were 7 different designs of solder pad. The resistors were placed in two placement directions along the x and y axes. Dimensions of the pads are defined in Figure 1 and Table 1.

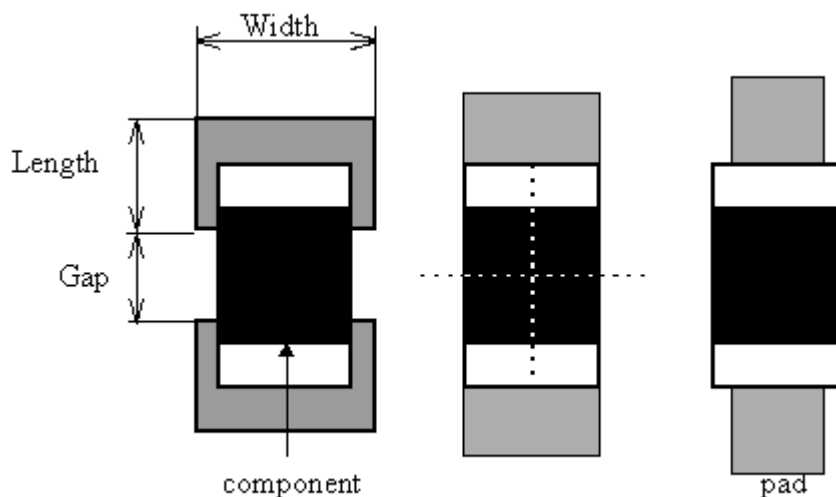


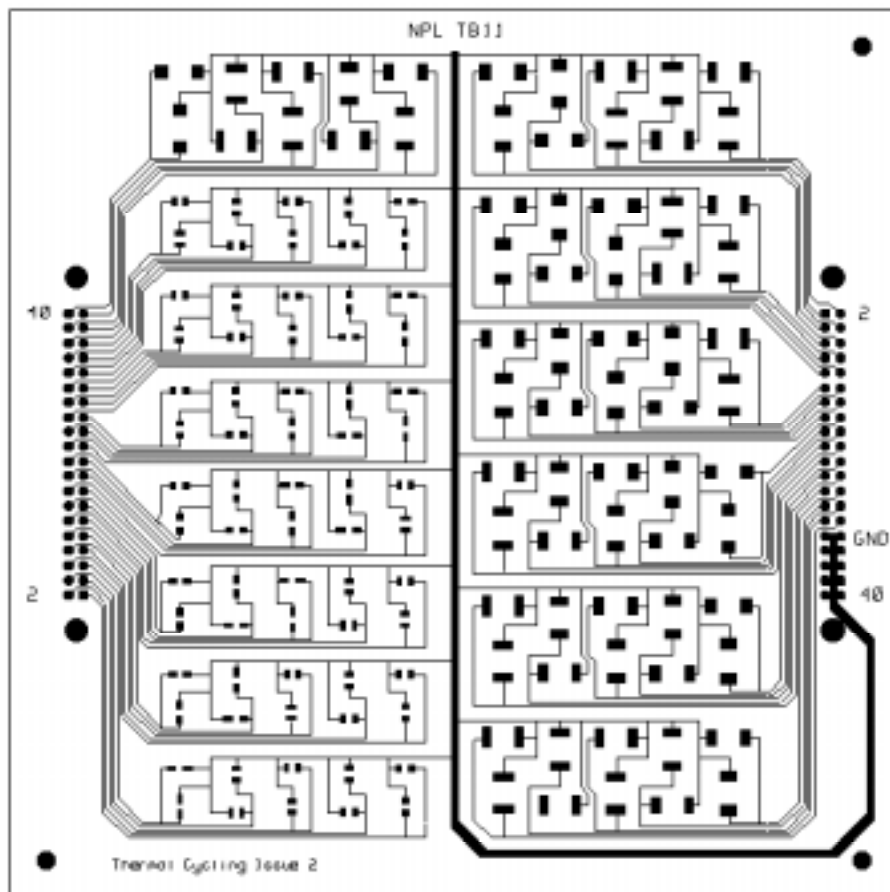
Figure 1 Definition of pad dimensions

Recommended size is D, based on IPC-SM-782. Area of pads is **constant, 1.62 mm^2 (0805) and 5.61 mm^2 (2512)**. The resistors were arranged in independent circuits on the PCB and could be electrically monitored individually using a multi-pole switching system and a digital voltmeter via two 40 way connectors on each board. The layout of the PCB is shown in Figure 2.

Table 1 Designed dimensions

<i>Resistors 0805</i>					
Design	Length [mm]	Width [mm]	Gap [mm]	Δ Length [%]	Δ Width [%]
A	0.94	1.73	1.02	-26%	36%
B	1.02	1.60	1.02	-20%	26%
C	1.12	1.45	1.02	-12%	14%
D	1.27	1.27	1.02	0%	0%
E	1.45	1.12	1.02	14%	-12%
F	1.60	1.02	1.02	26%	-20%
G	1.73	0.94	1.02	36%	-26%

<i>Resistors 2512</i>					
Design	Length [mm]	Width [mm]	Gap [mm]	Δ Length [%]	Δ Width [%]
A	1.52	3.68	4.01	-14%	17%
B	1.60	3.51	4.01	-10%	11%
C	1.68	3.35	4.01	-6%	6%
D	1.78	3.15	4.01	0%	0%
E	1.91	2.95	4.01	7%	-6%
F	2.03	2.74	4.01	14%	-13%
G	2.21	2.54	4.01	24%	-19%

**Figure 2 Board layout**

The PCB was single-sided FR4 with a photo-imageable solder resist and dimensions of 153x153x1.6 mm. All PCBs were from the same batch from a single manufacturer. The copper layer was 35 μ m thick with a HASL 63Sn/37Pb surface finish.

The base material of the resistors was a high purity (96%) alumina substrate. The termination of the resistors consisted of Pd/Ag inner layer, Ni barrier layer and Sn/Pb outer layer. All the resistors were from a single reel of components from a European manufacturer.

The assembly method was a simple single-sided reflow process of stencil printed solder paste. Components were placed using manual placement equipment. A single cartridge of paste (Multicore Sn63RP10AGS90) with low-residue flux was used. The stencils were manufactured from 0.10, 0.15 and 0.20 mm stainless steel. Apertures were laser cut. All assemblies were reflow soldered using the same profile in a convection reflow oven. The peak reflow temperature was 203°C and the maximum molten solder time was 58 s. The assemblies were left uncleaned.

2.2 THERMAL CYCLING

The assembled PCBs were inserted into a cycling oven for thermal cycling. The cycle (Figure 3) was selected on the basis of being representative of what is currently in industry use. There were two hold temperatures set, 120°C and -20°C with 10 minutes dwells.

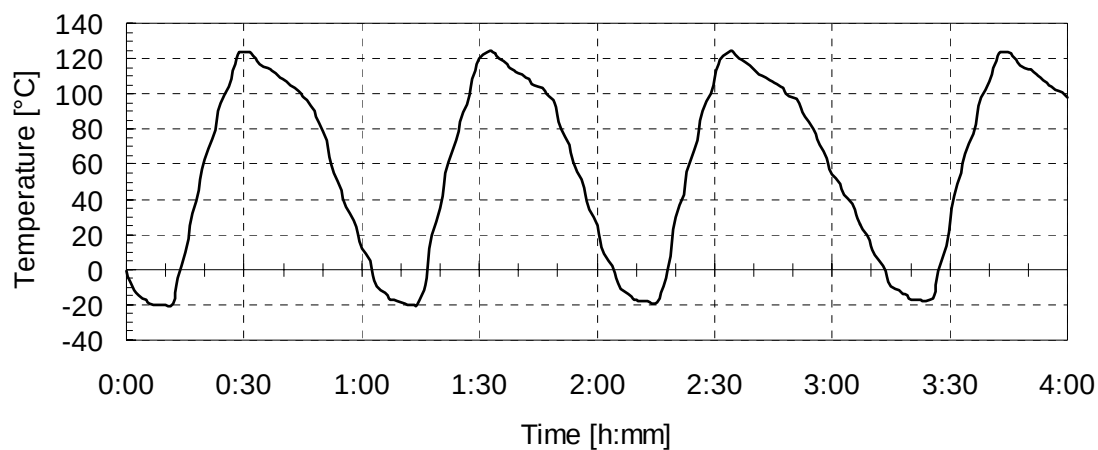


Figure 3 Temperature profile in the thermal cycling chamber (thermocouple attached to PCB)

2.3 RESISTANCE MEASUREMENT

After manufacturing of the PCBs, all resistors were electrically tested before thermal cycling. All the components exhibited an electrical resistance which was within the tolerance, $47000\ \Omega \pm 5\%$, $1000\ \Omega \pm 5\%$ for the 0805 and 2512 resistors respectively.

The resistance of each resistor was measured by the Voltage Method, where a constant voltage across a resistor is applied and the current through the resistor is measured. A range of 10 voltages was applied, and hence ten values of current were measured.

Table 2 Range of applied voltages

0805	[V]	0.60	1.00	1.70	2.90	4.80	8.10	13.6	22.9	38.6	65.0
2512	[V]	0.60	0.90	1.40	2.20	3.30	5.10	7.80	11.9	18.3	28.0

All resistors were periodically measured at room temperature. Each board was connected through two 40 way switch bridges to the measuring instrument.

2.3.1 Errors of Measurement

The measurement s error is considered here. We take here the largest likely to be encountered.

V-source:

In range of ± 110.00 V resolution step..... $\Delta V = 10$ mV

Operation point $V_0 = 11.9$ V

$$\text{Voltage relative error: } \delta V = \frac{\Delta V}{V_0} = \frac{10 \times 10^{-3}}{11.90} = 0.08\% \quad (2)$$

A-meter

In range of ± 100.00 mA resolution step..... $\Delta I = 10$ μ A

Operation point..... $I_0 = 11.9$ mA

$$\text{Current relative error: } \delta I = \frac{\Delta I}{I_0} = \frac{10 \times 10^{-6}}{11.90 \times 10^{-3}} = 0.08\% \quad (3)$$

Resistance:

$$\text{Relative error of resistance:..... } \delta R = \delta V + \delta I = 0.08 + 0.08 = 0.16 \% \quad (4)$$

Manufactured resistor tolerance:..... $\delta R'_1 = 1 \%$, $\delta R'_2 = 5 \%$,

Nominal value..... $R_1 = 47000 \Omega$, $R_2 = 1000 \Omega$

Absolute error of resistance:

$$\Delta R_1 = (\delta R + \delta R'_1) \times R_1 = 0.0116 \times 47000 = 545 \Omega \quad (5)$$

$$\Delta R_2 = (\delta R + \delta R'_2) \times R_2 = 0.0516 \times 1000 = 51.6 \Omega$$

From equation 5 for the absolute error of resistance we can estimate a limit which represents an open circuit for that particular resistor. For both 2512 and 0805 resistors, the open circuit value was considered to be 110 % (which is higher than total relative error of resistance measurement) of the nominal value, hence 1.1 k Ω and 49.45 k Ω respectively. If the resistance was higher than this limit a failure was found and marked.

2.4 RESULTS AFTER 2933 CYCLES

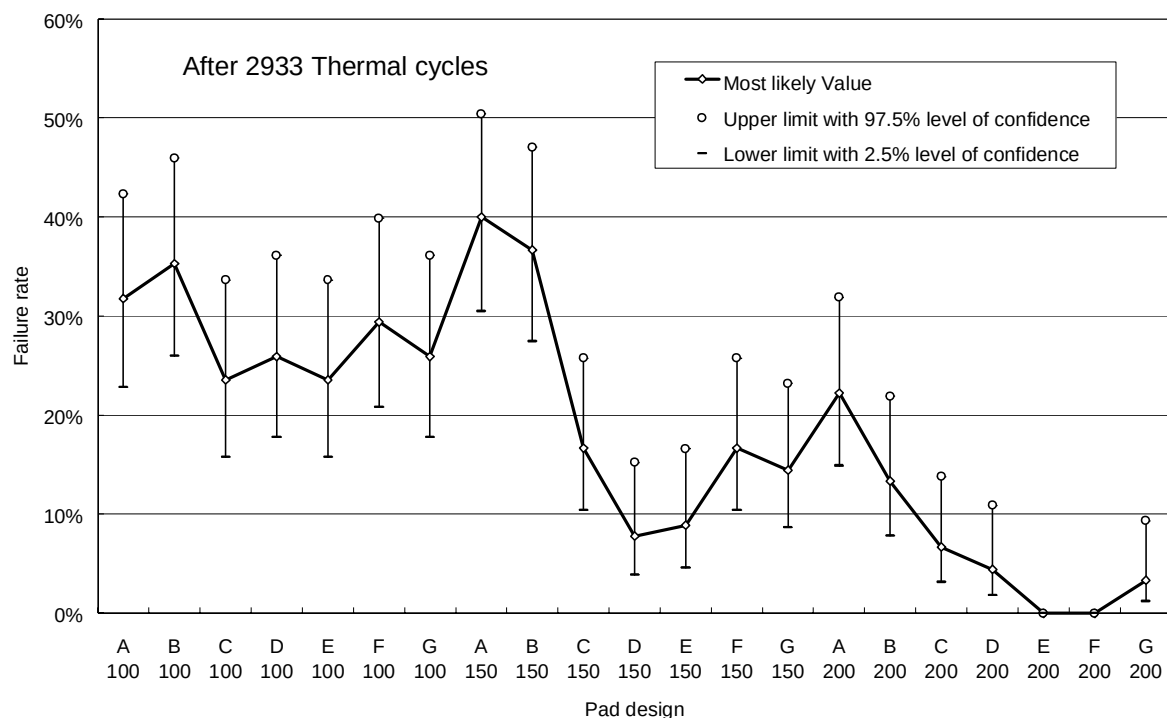
Only the 2512 resistors exhibited electrical failures. As mentioned above all resistors were periodically tested at room temperature. Table 2 contains data which shows how many 2512 resistors failed after a particular number of cycles. This is broken down further to the pad design and stencil thicknesses in Table 3.

Table 2 Number of failures after thermal cycling (2512 only)

Cycles No.	0	347	601	907	1195	1772	2202	2346	2570	2743	2933
Failures No.	0	0	0	2	3	49	123	189	271	301	338

Table 3 Most likely values of failure and their upper and lower deviation at 2933 cycles with 95 % confidence interval

Stencil Thickness [μm]	Design	Failures	Total	Most Likely Value [%]	Upper Deviation [%]	Lower Deviation [%]
100	A	27	85	31.8	+ 10.6	- 8.92
100	B	30	85	35.3	+ 10.6	- 9.32
100	C	20	85	23.5	+ 10.1	- 7.74
100	D	22	85	25.9	+ 10.3	- 8.11
100	E	20	85	23.5	+ 10.1	- 7.74
100	F	25	85	29.4	+ 10.5	- 8.62
100	G	22	85	25.9	+ 10.3	- 8.11
150	A	36	90	40.0	+ 10.4	- 9.52
150	B	33	90	36.7	+ 10.4	- 9.23
150	C	15	90	16.7	+ 9.06	- 6.27
150	D	7	90	7.78	+ 7.43	- 3.91
150	E	8	90	8.89	+ 7.70	- 4.27
150	F	15	90	16.7	+ 9.06	- 6.27
150	G	13	90	14.4	+ 8.75	- 5.77
200	A	20	90	22.2	+ 9.67	- 7.33
200	B	12	90	13.3	+ 8.57	- 5.50
200	C	6	90	6.67	+ 7.13	- 3.52
200	D	4	90	4.44	+ 6.43	- 2.63
200	E	0	90	0.00	+ 0.00	- 0.00
200	F	0	90	0.00	+ 0.00	- 0.00
200	G	3	90	3.33	+ 6.00	- 2.12

**Figure 4 Most likely value of failure rate with upper and lower deviation limits for different pad designs after 2933 thermal cycles**

The numbers of failures in Table 2 and 3 are cumulative and therefore if a resistor has failed earlier it is always counted as a failure. All cumulative numbers of failures represent damaged solder joints among 2512 resistors. The analysis did not find any failures among 0805 resistors. In Figures 5 to 7 show failure rate data for various cycle numbers.

2.4.1 Design and Stencil Thickness

It is apparent from Figures 5 to 7 that there is a difference in the number of failures for different designs and for different stencil thicknesses.

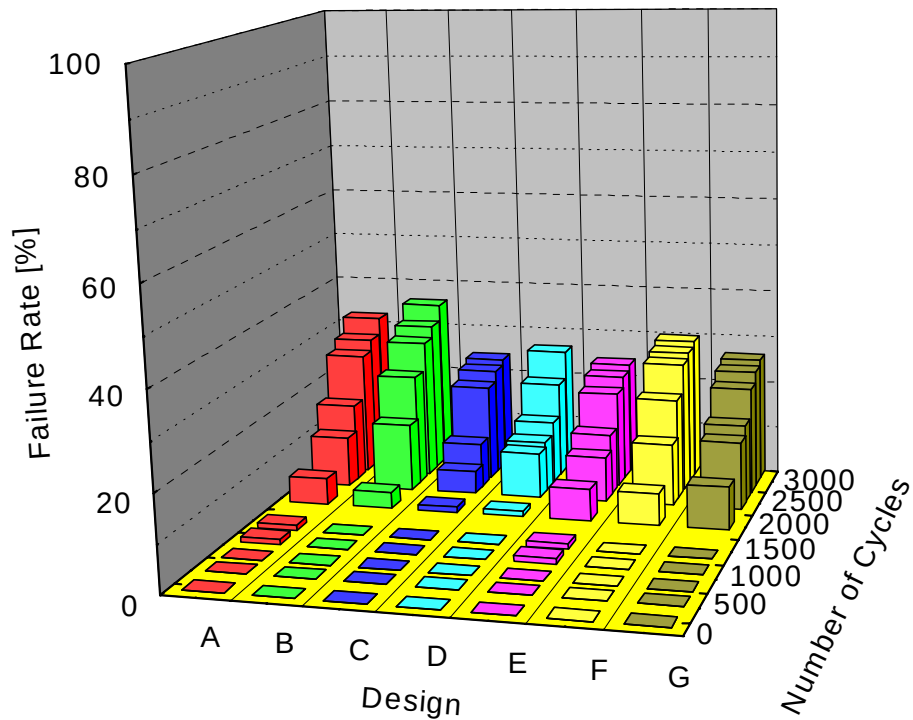


Figure 5 Failure rate for 2512 resistors made with 100 µm stencil thickness

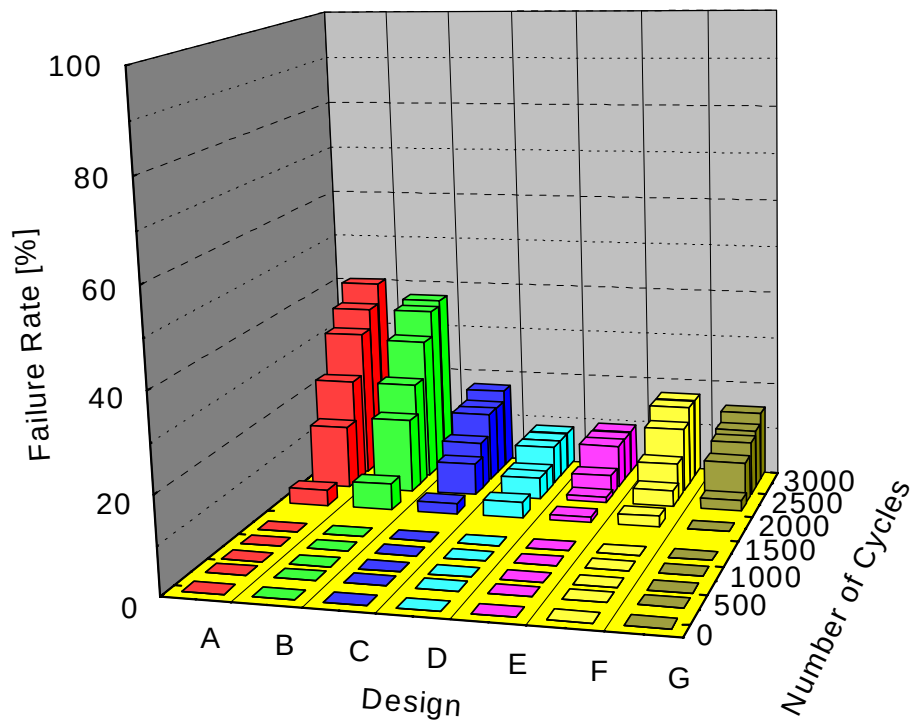


Figure 6 Failure rate for 2512 resistors made with 150 µm stencil thickness

The first failures occurred between 600 and 900 cycles for resistors manufactured with 100 μm stencil. Resistors manufactured with 150 μm stencil started to fail between 1200 and 1700 cycles. The last group of resistors manufactured with 200 μm stencil started to fail between 900 and 1200 cycles, although this is skewed by a single failure on one pad design.

Figure 5 shows that the smallest solder volume makes no big difference between the reliability of design types. All designs showed a similar number of failures. In Figure 6 (150 μm stencil) we can see that designs A and B perform significantly worse than C and G, whilst design D shows the best performance. It should be noted that D design is the closest to standard size (see IPC-SM-782). The failure rate with 200 μm stencil thickness is shown in Figure 7.

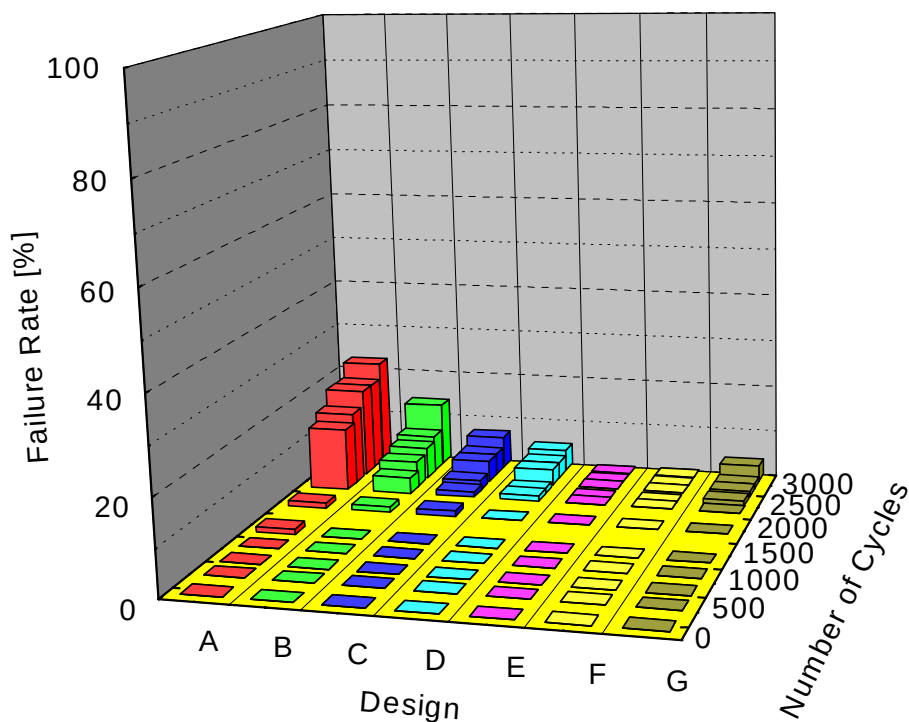


Figure 7 Failure rate for 2512 resistors made with 200 μm stencil thickness

The biggest solder volume exhibits the lowest number of failures overall as shown in Figure 8. Design A, the widest pad, is the worst case again, and designs E and F show the best performance.

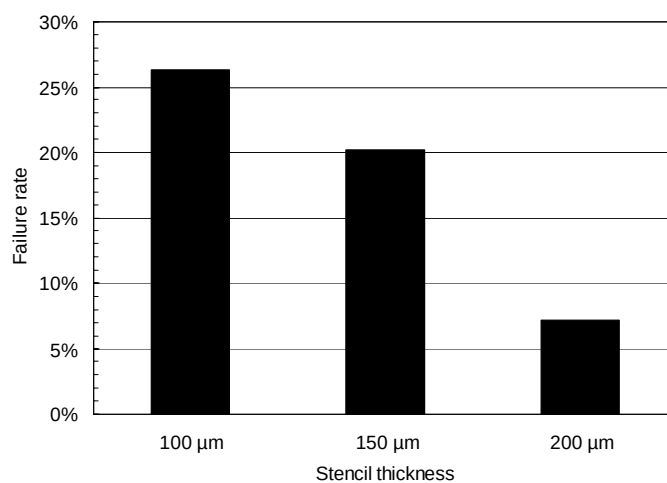


Figure 8 Failure rate for three stencil thicknesses after 2933 thermal cycles

It is apparent that the stencil thickness and hence solder volume has a big effect on the reliability. We can see that the higher the volume, the lower the failure rate. The higher solder volume probably performs better as a result of more solder in the solder fillet and hence a greater length for the crack to propagate through [1].

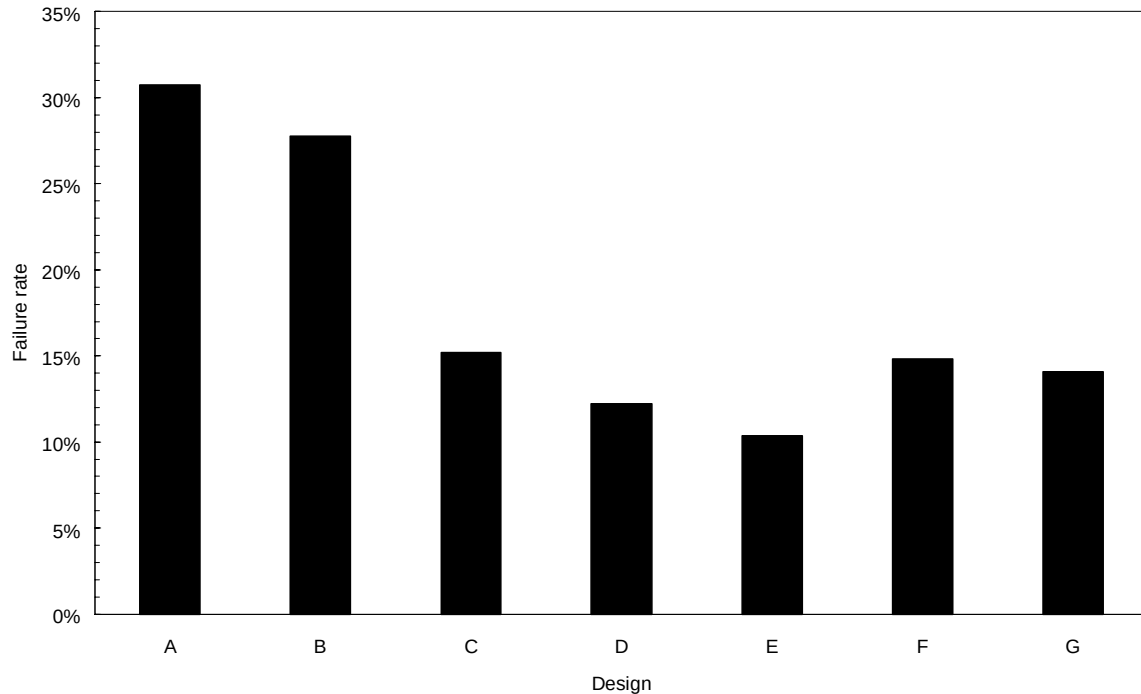


Figure 9 Failure rate as a function of pad

Figure 9 shows failure rate for all stencil thicknesses as a function of pad design. It is clear that D and E designs exhibit the best performance, and that that the A design has the worst performance.

2.5 CRACK SWITCH-ON VOLTAGE

As mentioned in section 2.3 there were a number of voltages used for measurement of resistance ranging from 0.6 V to 28 V for the 2512 resistors. The effect of scanning the voltage on cracked solder joints is investigated further here. Results on various joints of which some are shown in Figure 10, are investigated, and voltage curves are shown in Figure 11.

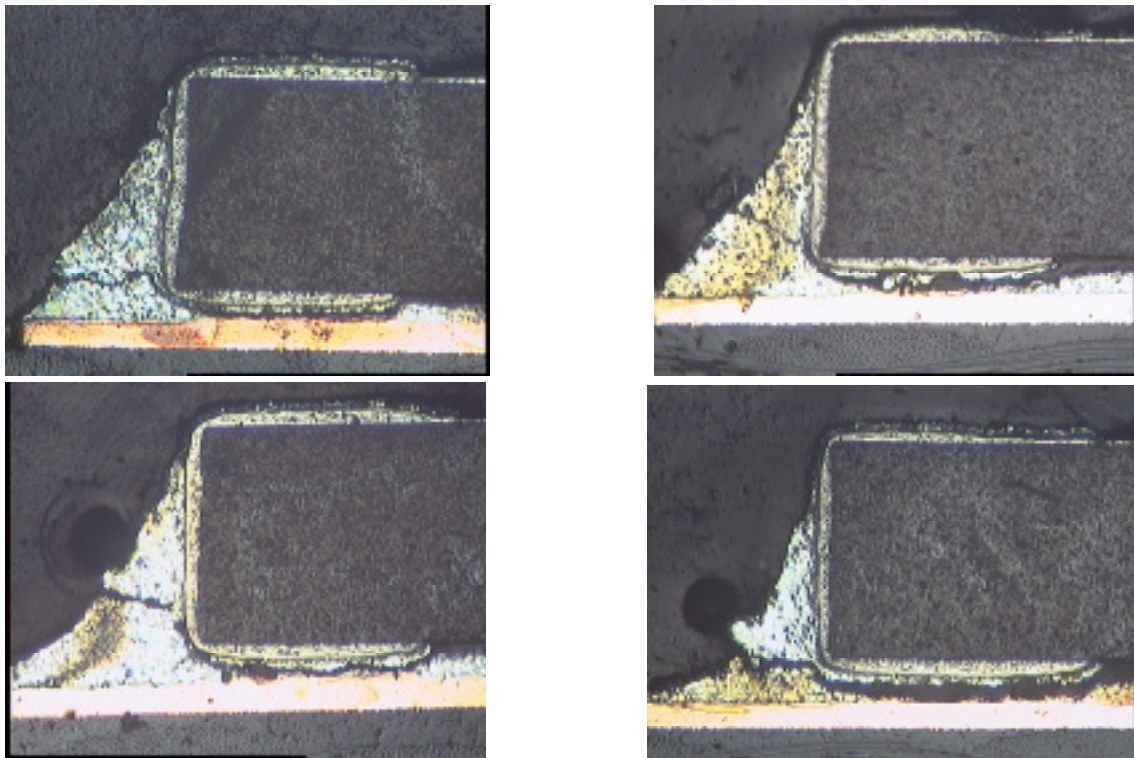


Figure 10 Cracks on the 2512 resistors

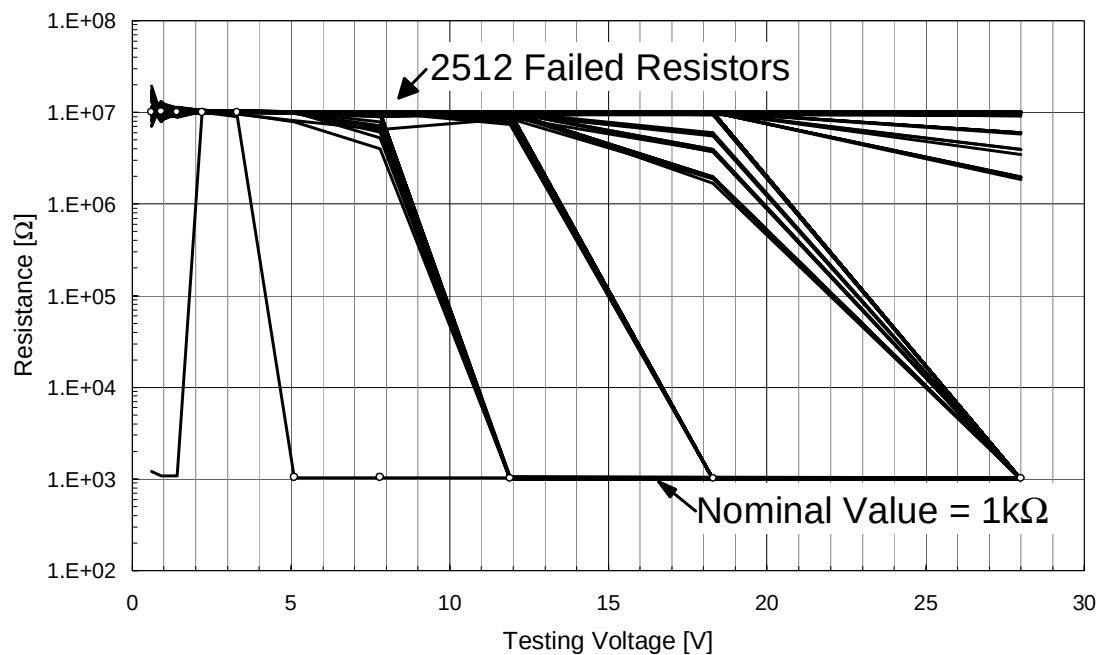


Figure 11 Switching-on voltage

A common feature of all the measurements is a sudden increase in current is, as the measurement voltage is increased, (cracks switch on). This is probably due to a current breakthrough effect Figure 11 value of **5 mA** is the recommended maximum limit for the measurement current. Above this current, breakthrough will occur and the detection of the crack will be missed.

2.6 FITTING OF WEIBULL DISTRIBUTION

This part of analysis was done to allow relative comparisons of resistor reliability as a function of stencil thicknesses and pad designs. To maintain the statistical integrity of the results from E and F designs with 200 μm stencil thickness were eliminated, as there were no failures at 2933 thermal cycles.

A modified Weibull distribution was fitted for all other solder pad designs. Equation 6 defines the Weibull distribution which is the mathematical interpretation of a wear-out fatigue mechanism.

$$F(n) = 1 - 2^{-\left(\frac{n}{N_f}\right)^\beta} \quad (6)$$

Where:

β = Weibull shape parameter

N_f = Median life to failure when $F(N_f) = 0.5$

n = Number of cycles

From β and N_f one can calculate the number of cycles to reach 1 % failure rate ($N_{1\%}$) which corresponds with the first failed resistor on an average electronic board with 100 resistors. An analysis [3] based on the Binomial distribution was done for 95 % confidence level of a result range for $N_{1\%}$, :see Table 4. Note there are no Weibull parameters predicted for design E and F at 200 μm stencil thicknesses, since there were insufficient failures to make a prediction.

Table 4 shows N_f and β values for the Weibull distribution and also includes the number of cycles for 1 % of the population to fail; for each of the stencil and pad design combinations. The Weibull parameters are useful for predicting failure rates at defined cycle numbers. The failure numbers in the last three columns are used later in Figure 16.

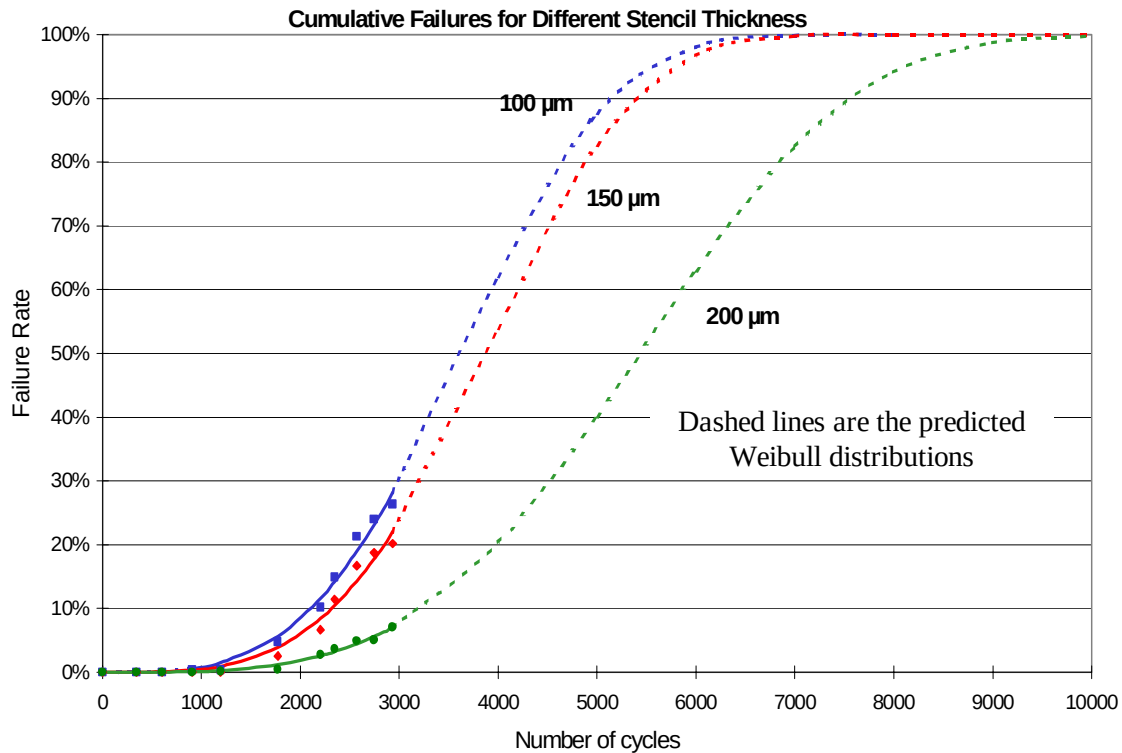
2.7 CUMULATIVE FAILURES FOR DIFFERENT STENCIL THICKNESS

Time development of cumulative failures (expressed as a function of the thermal cycles) for three stencil thicknesses are plotted in Figure 12. As described in the previous section the failure rate of a low volume solder joint increases faster than the higher volume joints.

In Figure 12 there are failure rates of different designs summed for the three stencil thicknesses. It is apparent that A and B types of pad designs have the worst performance.

Table 4 Results from Weibull function fitting

Thickness	Design	N _f	β	Most Likely Value	Lower Limit	Upper Limit
[μm]				N1%	N1%low	N1%up
100	A	3372	3.73	1084	772	1763
100	B	3240	3.61	1002	706	1657
100	C	3490	4.66	1408	1073	2077
100	D	3512	4.69	1423	1086	2096
100	E	3892	3.07	982	651	1772
100	F	3519	3.06	882	583	1596
100	G	3865	2.71	811	508	1584
150	A	3086	4.17	1117	824	1727
150	B	3184	3.61	985	694	1629
150	C	4287	3.30	1189	811	2061
150	D	6801	2.41	1178	697	2497
150	E	4666	3.98	1610	1171	2541
150	F	3901	4.23	1432	1061	2201
150	G	4081	4.25	1507	1119	2310
200	A	4018	2.96	962	628	1776
200	B	4125	4.82	1714	1318	2497
200	C	4789	4.72	1952	1493	2868
200	D	5062	4.90	2134	1649	3091
200	G	4116	9.10	2585	2249	3155

**Figure 12 Development of cumulative failures rate for different stencil thicknesses**

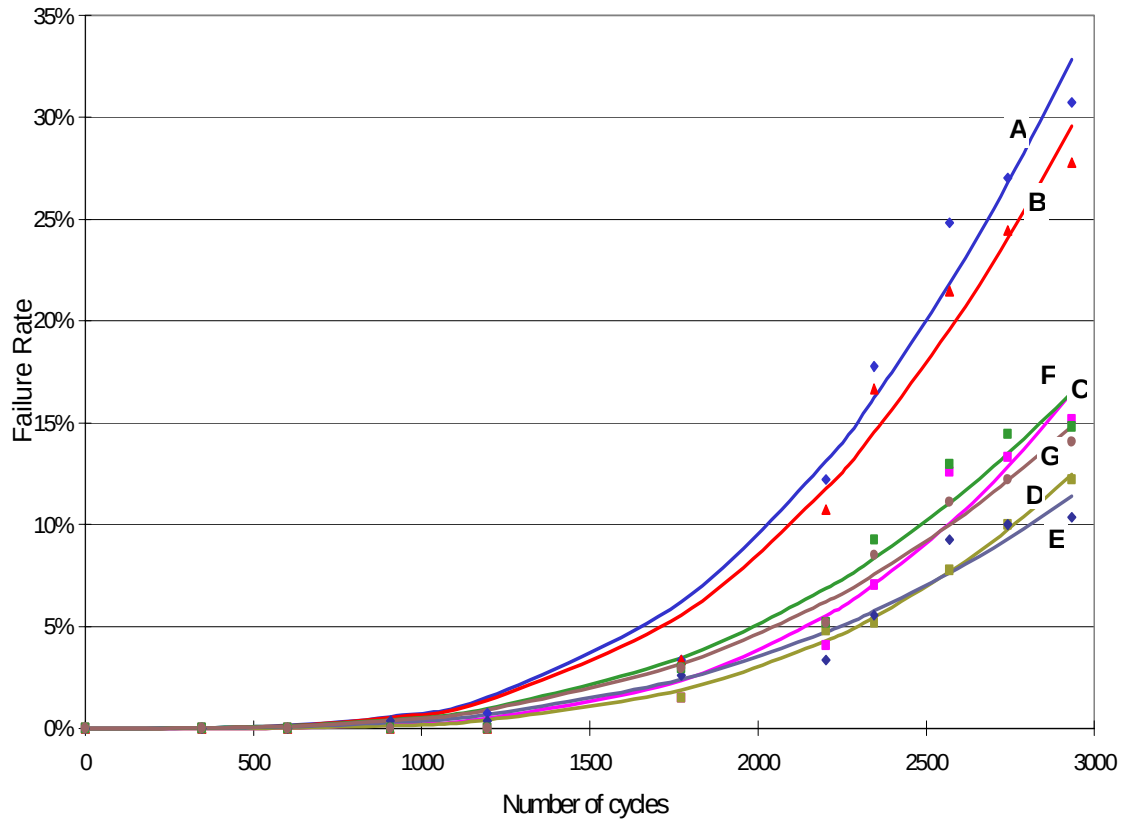


Figure 13 Development of cumulative failures rate for different pad design

2.8 CUMULATIVE FAILURES FOR DIFFERENT DESIGN

In this section the development of failures based on pad design is reviewed. The failure rate for A and B designs develop faster than the D and E designs. Figures 14 and 15 show the developments of failure rates for the worst (A design) and the best (E design) type of pad design for the three stencil thicknesses. It is clearly apparent that the failure rate of A design increased more rapidly than the failure rate of E design and reached 1 % of failures within 1195 thermal cycles.

Note that the 100 μm stencil thickness exhibits better results than 150 μm thickness with the A design which may be caused by random statistical error at the lower failure rate.

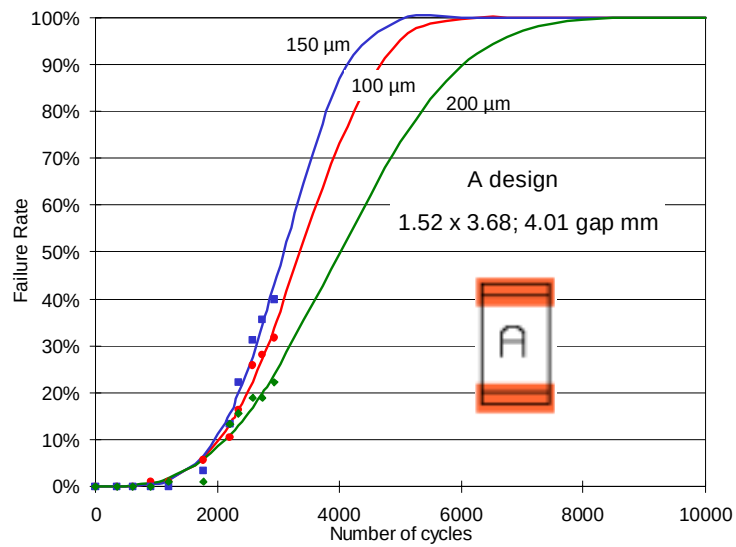


Figure 14 Development of cumulative failures rate for A design

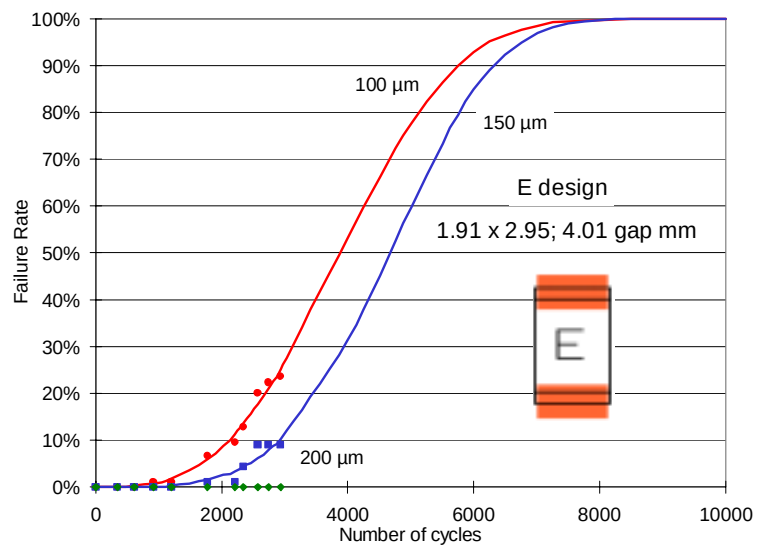


Figure 15 Development of cumulative failures rate for E designs

2.8.1 Hodograph

The number of cycles to reach 1 % failure rate for each design & stencil thickness is plotted in Figure 16.

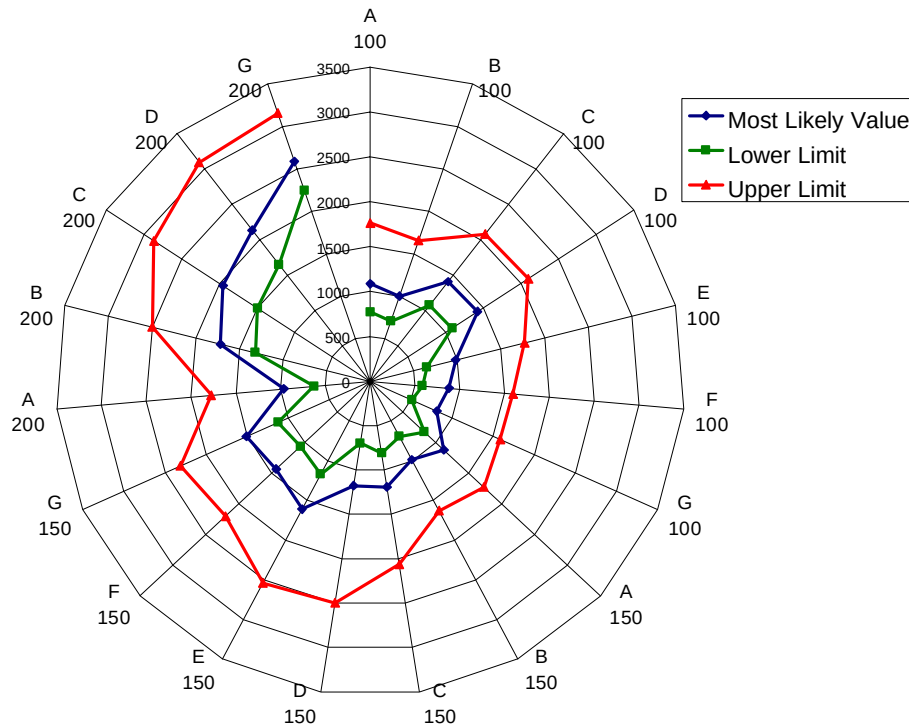


Figure 16 Hodograph of number of cycles to 1% failure rate with upper and lower deviation limit (for values see Table 4)

This plot contains a great deal of information, and depicts the influence of pad design and stencil thickness. The hodograph readily shows the interaction between these two parameters. The graph shows reduced number of failures as the stencil thickness increases and the improvement in performance with pad design D (standard design). It is also clear that design A is worse than design E, i.e. a short fat pad is worse than a long thin pad.

2.9 IN-SITU MEASUREMENTS

As mentioned previously all measurements were taken at room temperature. The PCBs were removed from the oven and resistance was then measured. To investigate the behaviour of resistors and their solder joints in the oven during the thermal cycling, additional in-situ measurements were carried out.

These measurements were carried out on 40 selected 2512 resistors, 20 of which had exhibited a failure in the past and another 20 that had not failed.

2.10 RESULTS FROM IN-SITU MEASUREMENT

The resistance values during thermal cycling for a previously failed resistor are shown in Figure 17. It is clear that the resistance is not stable, with its shifting between being connected, and being open circuit. This transition depends on the instantaneous temperature.

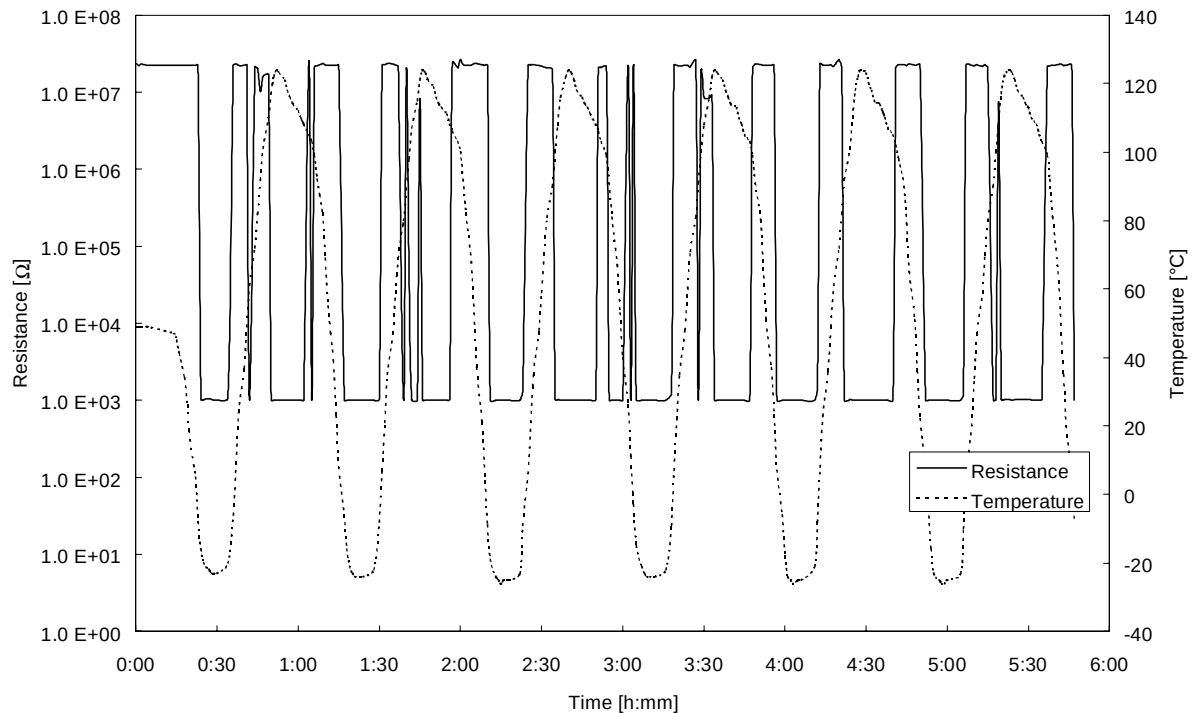


Figure 17 Results from measurement during thermal cycling

Two important observation are made:

1. If the temperature is at a maximum or minimum dwell in the cycle there is a continuity connection across the solder fillet.
 - If there is a temperature gradient, there will be creep between the two halves of the crack, which will cause intermittent contacts.
2. The contact is randomly switched on/off during the temperature ramp in the cycle.
 - During the high and low temperature dwells the crack is temporarily repaired and continuity achieved.

2.11 FAILURE RECOGNITION PROBABILITY

With the DC constant voltage measurement method there is no guarantee that a cracked resistor will be fully disconnected when at the measurement is taken. This is particularly significant for periodical measurements outside the thermo-cycling oven at room temperature. As explained earlier the number of failed resistors changed with the temperature gradient. If we measure at room temperature, we should know what is the probability that the resistors exhibit failures.

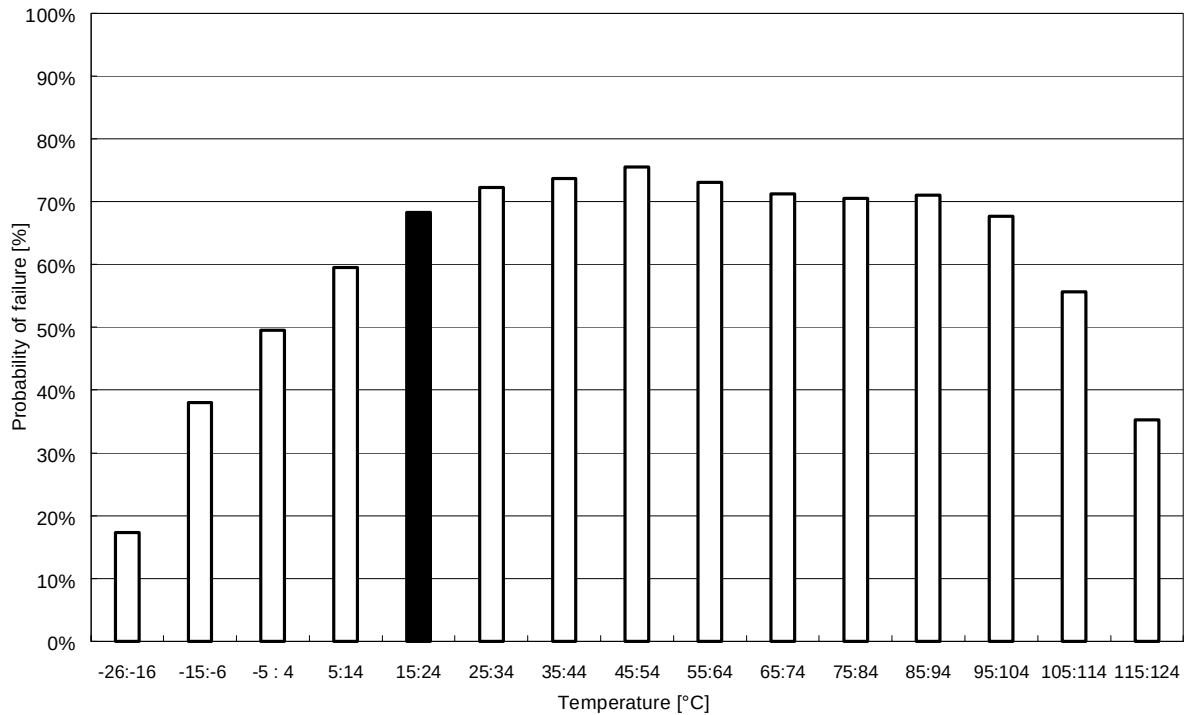


Figure 18 Probability of recognising of the failure in the solder joint with respect to the temperature

In Figure 18 the probability of recognising known failures is shown. The probability of failure is the ratio of measured failures against the 20 resistors previously known to have failed in this sample, for each of the temperature ranges. This was done over 40 cycles. It is apparent that highest probability of the failure recognition is between 45 and 54 °C. In this part of the cycle the temperature changes most rapidly and there is the biggest temperature gradient and the solder joint is under the greatest load.

3. CONCLUSIONS

The effect of component size was very marked with no failures with the 0805 resistors, up to 3000 cycles. Hence pad design and stencil thickness were not found to be important with the 0805's. However with the 2512 resistors there were a number of failures, and now the pad design and stencil thickness were critical.

The effect of stencil thickness was important. Using the 100 μm stencil there was little influence of pad design, and hence we can conclude there is a critical solder volume for good reliability, and that was not achieved in this specific case. For 150 μm stencil there was a clear effect of pad design, but the best reliability was achieved with the 200 μm stencil. For the 200 μm stencil there were no failures for pad designs of D & E. Hence a conclusion of this work is that more solder is good, as long as the wetting and reflow of the joint is maintained. A larger volume increases the cross-sectional area of the joint, and this is the beneficial effect, by virtue of increasing the crack length to failure.

The effect of pad design with the 2512 resistors was very critical with the 150 μm stencil. Pad design A had the poorest performance, which was the short fat pad. Stretching the pad, as in design E was less harmful. These results are important as designers are often pushed, due to space limitations, to alter pad designs towards the A design. Where solder volumes are critical this will have an adverse effect on reliability.

For DC resistance measurements it was found that above 5 mA there is a phenomenon of current breakthrough when measuring cracks. It is recommended that for reliable detection of cracks, test currents of less than 5 mA be used.

In-situ measurements of resistance revealed that the resistance of cracked joint is unstable during cycling. Usually the resistance is at a minimum at either end of the temperature extremes of the thermal cycle, but there is random fluctuation during the ramp between the temperature holds. This is significant in terms of measurements of the assemblies when they are removed from thermal cycling chamber.

ACKNOWLEDGEMENTS

The work was carried out as part of a project in the Reliability of PCB Assemblies (MMP8) Programme of the UK Department of Trade and Industry. The authors are grateful for useful discussion with E. R. Wallach and J. Warde from Department of Materials Science and Metallurgy University of Cambridge.

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