

REPORT

Draft NPL SIR Measurement Procedure

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ABSTRACT

The method detailed in this report has evolved from studies here at the NPL. Starting from existing standards, such as ISO, IPC and Bellcore. We have developed a test that is more realistic in determining circuit reliability than has hitherto been published by the above organizations. These organizations are currently reviewing their procedures, and this document contributes to this advancement.

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Approved on behalf of Managing Director, NPL, by Dr C Lea,
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1. General Description

The Surface Insulation Resistance (SIR) technique has been widely used to assess the effect of contaminants on the reliability of assemblies. The SIR measurement technique, compared with other methods, has the advantage that it can be used to detect localized contamination, and that it can be used to measure the effect of contaminants, both ionic and non-ionic, on the reliability of the printed circuit assemblies. The sensitivity and the ability to measure at specific locations, allow the SIR technique to identify the originating process causing the observed contamination. Therefore, on a single board where there have been several assembly processes, SIR measurements may be able reveal the effect of specific assembly processes. The SIR technique is used to characterize the effect of the different fluxes, pastes, solder wires and production processes on the reliability of the board. SIR measurements are carried out in controlled environments for a specified time, with specified bias.

There are two different test boards available, depending on the evaluation requirement. The test board, NPL TB2 (see Figure1) with two comb patterns, can be used for assessing different fluxes. The same test board can also be used for assessing solder paste, and includes the option of placing two QFPs and seven 0805 capacitors.

For assessing the different production processes, NPL TB2 or IVF-2A (see Figure2) can be used. The boards are then assembled by the company using its own production process. NPL TB2 is a single sided surface mount assembly and the IVF-2A board is a mix technology assembly and can accommodate reflow soldering, wave soldering and solder wire soldering.

The following SIR measurement procedure details the steps for assessing the effect of different fluxes, pastes, and production process on circuit reliability.

2. Materials and Apparatus Requirements

2.1 Boards

- a) The test board (NPL TB2) for assessing different fluxes is shown in Figure1. The two comb patterns in the board shall be fluxed with the test flux.

- b) The same board (NPI-1B2) can be used for testing different pastes. The two QFP and seven 0805 capacitors footprints shall be printed with the test paste
- c) The test board (IVF-2A) is shown in Figure 2. The components on the top side of the board are used to assess the reflow soldering process, and the components on the bottom side of the board and the through hole components are used to assess the wave soldering process. The through hole components can also be used to assess the solder wire soldering process.

2.2 Cables

Halogen-free 0.05 in. pitch cable with 34 conductors. Configuration suitable for wiring the board.

2.3 Connectors

0.1 in. pitch single sided, 32-way gold connector

2.4 Solder wire

very Low flux residue solder wire

2.5 Drying oven

Suitable for use up to $130^{\circ}\text{C} \pm 3^{\circ}\text{C}$.

2.6 Reflow oven

It is recommended that a reflow oven with temperature profiling capability is used.

2.7 Soldering iron

2.8 Humidity chamber

Capable of programming environments up to 90°C with temperature control of $\pm 0.2^{\circ}\text{C}$ and relative humidity up to 90% with control of $\pm 5\%$ at a specific RH. The chamber should be constructed with stainless steel inner surfaces and be well insulated. The temperature and humidity measurements should be taken using sensors such as dry and wet bulb thermometers. Solid state sensors cannot tolerate high temperature and humidity. The temperature humidity levels of the test chamber shall be recorded throughout the test, preferably with independent control sensors.

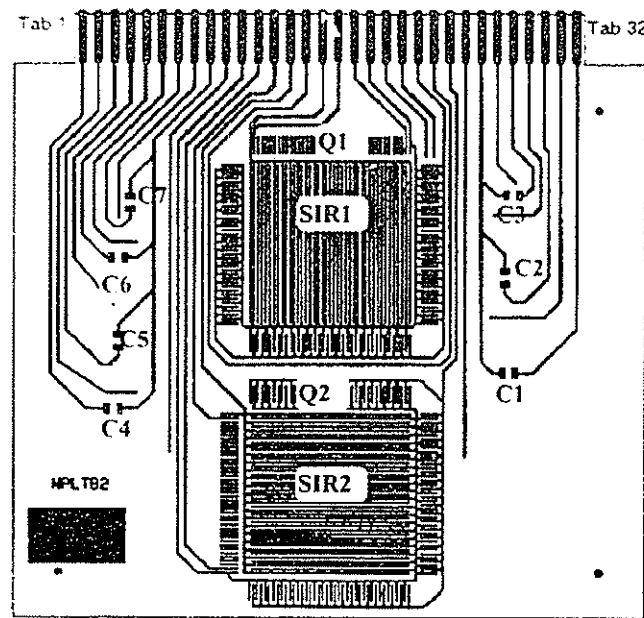


Figure 1 The test board for assessing the different fluxes and pastes (NPL TB2)

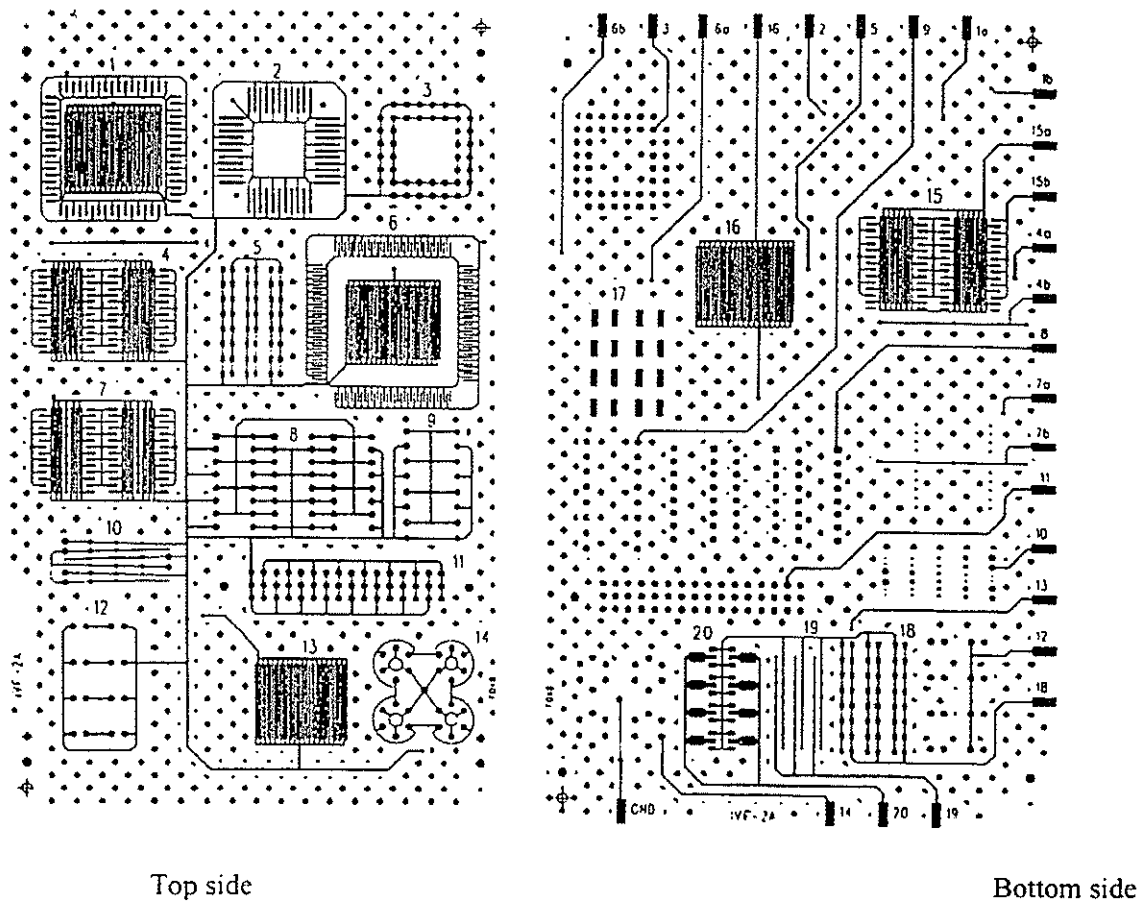


Figure 2 Lay-out of the test board for assessing the different soldering processes (IVF-2A)

2.9 High resistance measurement system

The measurement system shall comprise

- a) A measuring device capable of measuring surface insulation resistance (SIR) in the range of 10^6 ohms to 10^{12} ohms.
- b) A test and bias voltage supply capable of providing 5 volts dc ($\pm 2\%$) with a one megohm load.
- c) A sample selection system capable of individually selecting all the test patterns in the measurement experiment. The system shall incorporate a one megohm current limiting resistor in each current pathway.
- d) The tolerance of the total measurement system shall be $\pm 5\%$ up to 10^{10} ohms, $\pm 10\%$ between 10^{10} to 10^{11} ohms, and $\pm 20\%$ above 10^{11} ohms.
- e) The measurement system shall be calibrated by substituting a calibration board (2.10) in place of the test coupons in the chamber at ambient conditions.
- f) The data sampling rate should be every ten minutes.

2.10 Calibration board

Calibration of the complete system using a calibration board with known resistors shall be carried out every three months. The calibration board is shown in Figure 3. The calibration board shall be of the same dimensions as the test board with one of each 10^6 , 10^8 , 10^{10} and 10^{12} ohm resistors in specific current pathways.

2.11 Test board holders

There are two types of holders. One is an arrangement of equally spaced (minimum of 15 mm) edge connectors (2.3) mounted on a stainless steel frame for NPL TB2 test boards. The other is a simple stainless steel frame accommodating IVF-2A test boards with equal spacing (minimum of 15 mm).

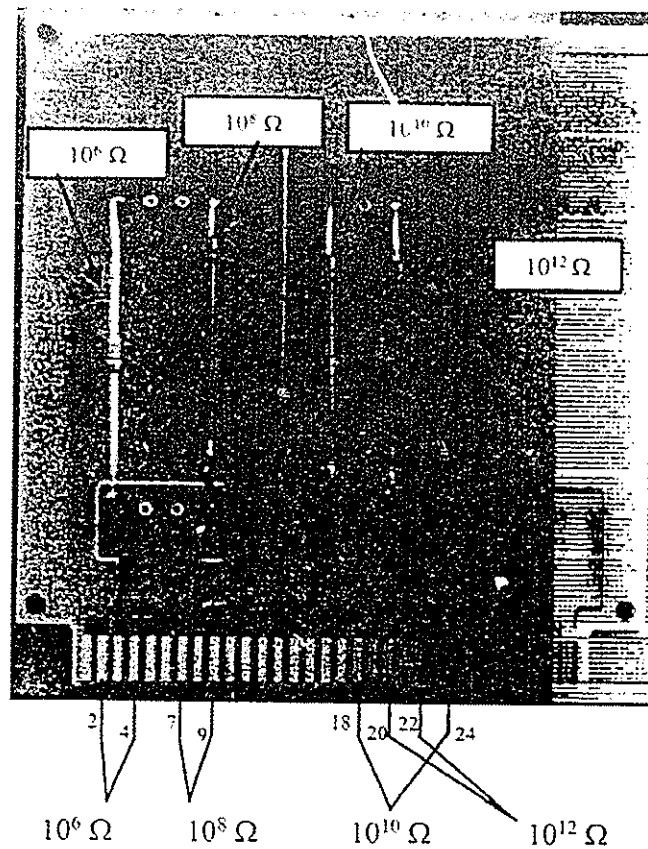


Figure 3 The calibration board

3. Test Procedure

3.1 Preparation of the test boards

3.1.1 Preparation of test board for testing different fluxes and pastes

a) Clean the test board and assess the cleanliness of the board

(1) Hold the board vertically and spray de-ionized water for 10 seconds, then spray with IPA for 10

seconds. Bake the test board in the oven for 16 hours at 125°C.

(2) An alternative cleaning method. Place the test board in an ionic contamination tester containing 75% v/v propan-2-ol, 25% deionized water solution, and process until the measurement indicates an ionic residue less than $0.1 \mu\text{g}/\text{cm}^2$ NaCl equivalent

- (3) Set up clean boards in the humidity chamber, by insertion into the edge connector arrangement.
- (4) Take an initial SIR measurement @ 23°C/50%RH (room conditions).
- (5) Take SIR measurements every 10 minutes during 16h exposure @ 65°C/85%RH.
- (6) If the SIR value is stable and greater than 10¹¹ ohms the boards are satisfactory for fluxing and printing. If the SIR does not meet this criteria, the boards should be rejected.

b) Fluxing the test board

- (1) Flux the test board at room temperature with 50 µl flux. The flux concentration will be recommended by the flux manufacture. The control board is not fluxed.
- (2) Dispense the flux slowly in a number of drops initially onto the centre of the comb pattern and ensure a uniform coverage by dispensing further drops in areas of low coverage. The aim is to achieve a uniform thickness of the flux over the SIR pattern. The flux may spread outside the pattern.
- (3) Flux drying condition. Lay the board flat in a fan oven at 100 °C for 5 minutes.

c) Printing the test board

- (1) Print the board with test paste. The control board is not printed.
- (2) Using a 100 µm stencil (NPL Sten TB2) print the paste onto the two QFP and seven 0805 capacitors' footprints.
- (3) Solder the test board using a reflow solder oven with a standard temperature profile or a profile recommended by the paste manufacture.

3.1.2 The test board for assessing the different production processes

The test board for assessing the different production processes, is tested directly in the as-received condition, and no preparation is required.

3.2 Method for connecting the test board to the SIR measurement system

The connections from the test patterns which come out on the tabs for NPL TB2 and IVF 2A boards are listed in Table 1 and Table 2 (see Figure 1 and Figure 2 also)

Table 1: Tab connections to board NPL TB2

Test pattern	Identification	Tab connection
Comb pattern 1	SIR1	16
Comb pattern 2	SIR2	14
QFP footprint 1	Q1	22
QFP footprint 2	Q2	24
0805 capacitor footprint 1	C1	32
0805 capacitor footprint 2	C2	30
0805 capacitor footprint 3	C3	28
0805 capacitor footprint 4	C4	1
0805 capacitor footprint 5	C5	3
0805 capacitor footprint 6	C6	5
0805 capacitor footprint 7	C7	7
	Bias	9, 11, 19, 26
	Earth	2, 4, 6, 8, 10, 12, 13, 15, 17, 18, 20, 21, 23, 25, 27, 29, 31

Table 2 The connections to IVF-2A board

Test pattern	Connection	Soldering method
Solder pads to PLCC68	1b	reflow
Comb within footprint for PLCC	1a	reflow
Surface mount socket for PLCC	2	reflow
Through hole mount socket for PLCC	3	wave
Solder pads to reflow soldered SO28 without via hole	4b	reflow
Comb within footprint for reflow soldered SO28 without via hole	4a	reflow
Reflow soldered 0805 chip capacitors	5	reflow
Solder pads to QFP	6b	reflow
Comb within footprint for QFP	6a	reflow
SO28 with 0.5 mm via hole beneath		
Solder pads to reflow soldered SO28 with via hole	7b	reflow
Comb within footprint for reflow soldered SO28 with via hole	7a	reflow
Axial resistors	9	wave
Via hole section	10	reflow
Through hole mount connector	11	wave
Reflow soldered free comb	13	reflow
Solder pads to wave soldered SO28	15b	wave
Comb within footprint for wave soldered SO28	15a	wave
Wave soldered free comb	16	wave
Wave soldered 0603 chip capacitor	18	wave
Wave soldered 0805 chip capacitor	19	wave

Two methods can be used for connecting the test board to the SIR measurement system. Do not handle the boards with bare hands, wear clean-room gloves and only handle edges.

- a) Slide test board edge into the connector (2.3)
- b) Carefully hand solder the cable (2.2) to the termination of the test patterns on the board. The board should be protected with aluminum foil during soldering, and very low flux residue solder wire used. The solder joints should be cleaned using a cotton pad with IPA.

3.3 *SIR measurement procedure*

3.3.1 Sample size

Three test boards and one control board for each test. The control board shall be cleaned (3.2. a)) but not fluxed, printed or assembled.

3.3.2 SIR measurement for test board

- a) High resistance measurement system calibration. Prior to connecting the test board to the measurement system, the calibration board (2.10) shall be connected to the system and a measurement taken. If any channel does not read within the tolerance value of the total measurement system ($\pm 5\%$ up to 10^{10} ohms, $\pm 10\%$ between 10^{10} to 10^{11} ohms, and $\pm 20\%$ above 10^{11} ohms), then this must be rectified. If the cleanliness of the connector is suspect, this can be cleaned or replaced. If the accuracy of the instrument is suspect, calibrate with standard resistors
- b) Test board measurements. Carefully mount the test boards vertically in the humidity chamber and connect the wiring loom from the boards to the outside measuring chamber without bias applied.

A single test voltage of 5V should be used throughout the entire experiment. If an automatic monitoring system is used, start the monitoring at room temperature, and use a 20 minute cycle time.

The test conditions should be 65°C and 85%RH. The temperature should be ramped up first and allowed to equilibrate, before the humidity is increased. The humidity should be brought up slowly enough to avoid condensation on the board. This may be best achieved by bringing the humidity up to 75%RH, with a small hold and then a further increase to 85%RH. The temperature and humidity of the chamber should be checked with calibrated instruments. The

test period is 168 hours. The acquired data should be stored for future trend analysis and for the development of pass fail criteria.

4. Assessment

If a board exhibits intermittent electrical failure or anomalous performance during SIR testing, carry out visual inspection for the presence of dendrite formation or corrosion products. SEM/LDX analysis shall be carried out where necessary, and the following conditions recorded.

- a) Presence of dendrites and corrosion products. If present, count and record the number of dendrites. A dendrite should only be counted when its length exceeds 200 μm . Multiple dendrites in a cluster that are interconnected should only be counted as one dendrite. Record the percentage of the spacing between the conductors bridged by the worst-case corrosion products. A picture or SEM image for the tested sample shall be taken.
- b) Presence of discolouration between conductors (discolouration on conductors is acceptable). If present, discolouration shall be recorded as a colour image and included in the test report.

If the resistance measurements taken on the control boards fall below 100 G Ω and the test boards with the candidate material fail, a new control and test boards must be prepared and the test repeated.

Any reason for deleting values (scratches, condensation, solder bridged conductors, outlying points, etc.) must be noted. Rejection of results for more than 2 test patterns for a given condition shall require the test to be repeated.

5. Test Report

The test report shall include, as a minimum, the following information:

- a) Identification and preparation of the flux and paste samples. The flux concentration must be recorded.
- b) Test conditions; temperature, humidity and bias voltage.
- c) Details of the production process used by the company.

- d) The Individual charts or graphs showing the average log SIR value with time for three test boards and a control board, the standard deviation should be given as well.
- e) The number of dendrite and the percentage of corrosion products formed during the SIR test.
The picture or SEM image of the discolouration between conductors for the test boards.
- f) Simple explanation and conclusion about the test results.